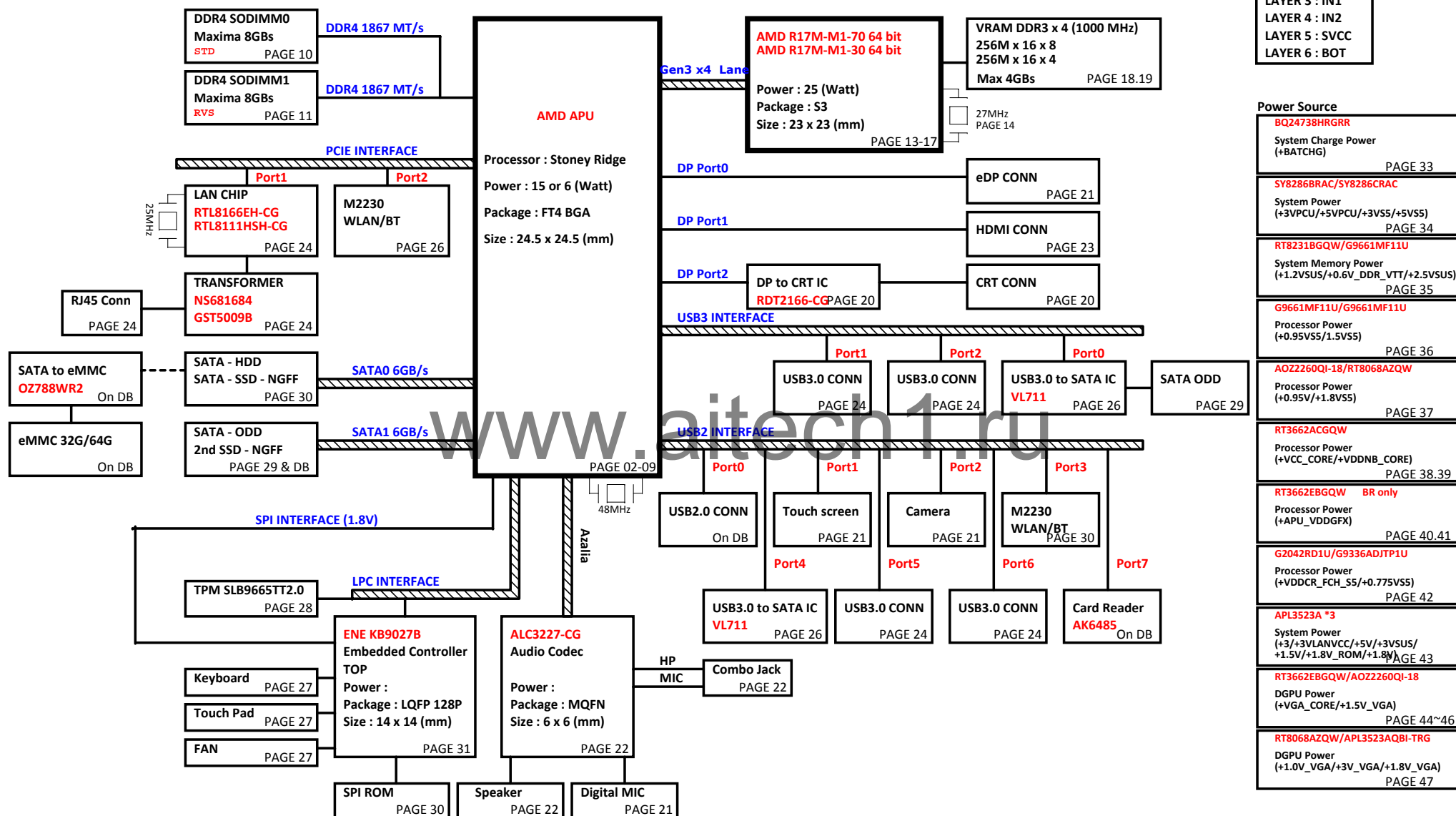
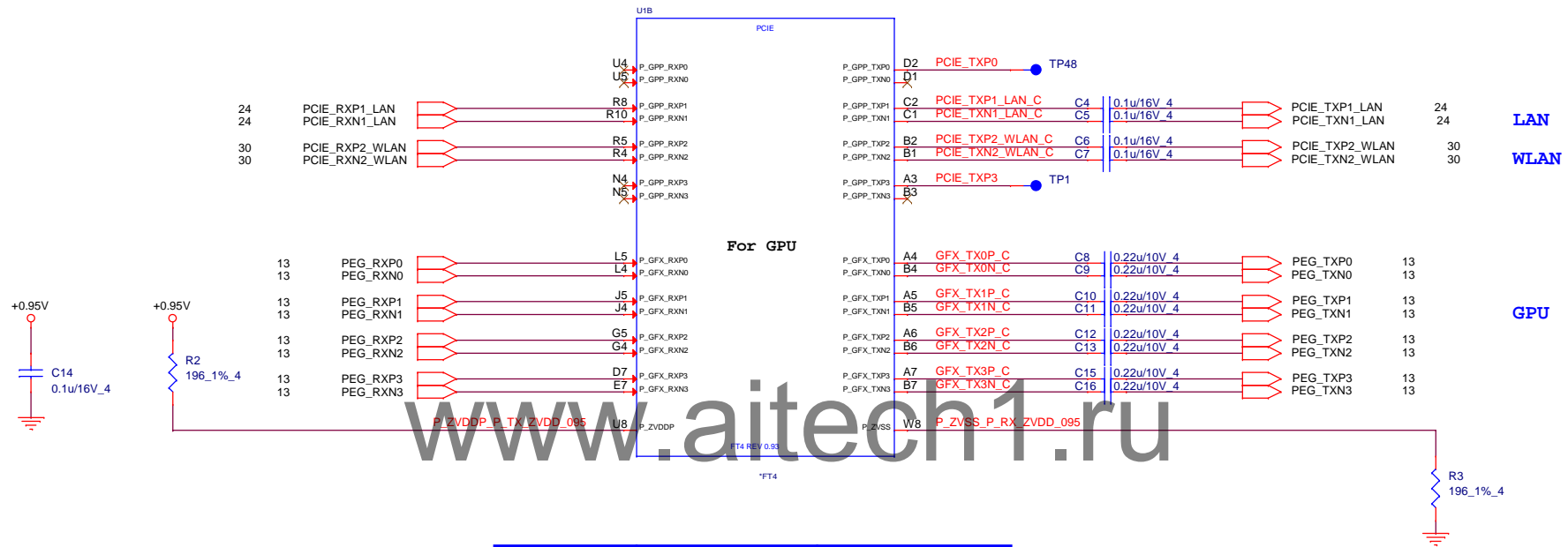


NFL-C 14" AMD SR FT4 DIS/UMA Block Diagram



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

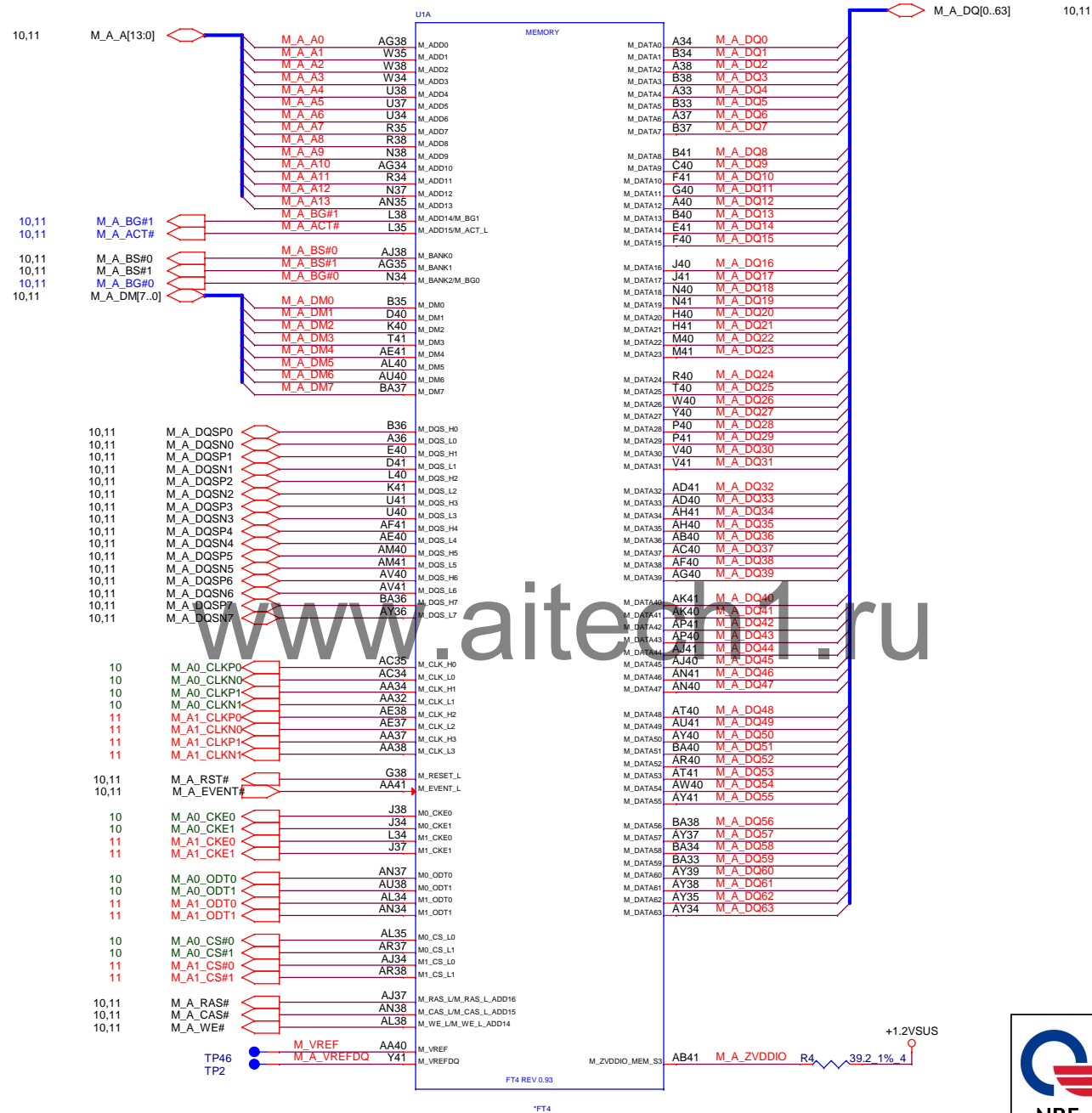


	QBCON PN	TOP BSQ
A9-9420	AJ094208T02	AJ094208T01
A6-9220	AJ09220RT01	AJ09220RT00
A4-9120	AJ09120UT01	AJ09120UT00
A6-9200e	AJ00920UT01	AJ00920UT00
E2-9000e	AJ900EAVT01	AJ900EAVT00



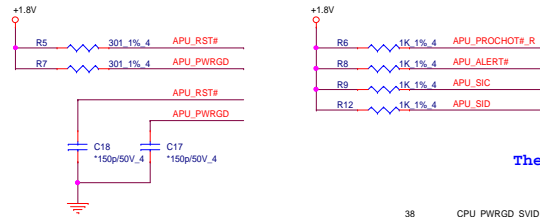
PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

Size	Document Number	Rev
	ST 17(PCIE)	1A
Date: Wednesday, March 08, 2017	Sheet 2 of 48	



PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

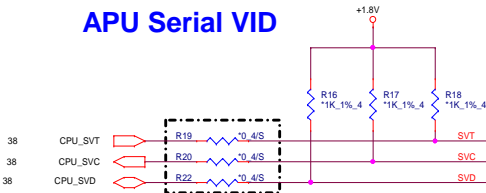
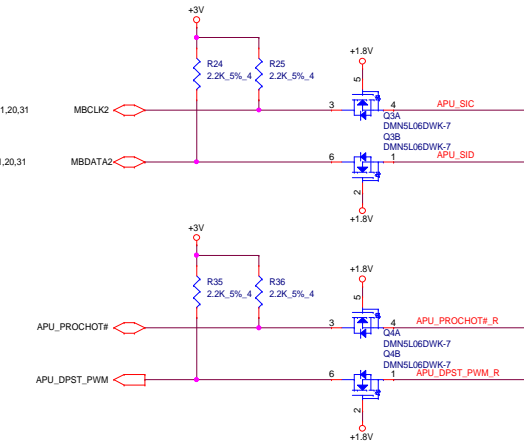
Size	Document Number	Rev
	ST 277(MEM)	1A
Date: Wednesday, March 08, 2017		Sheet 3 of 48



Thermal Sensor

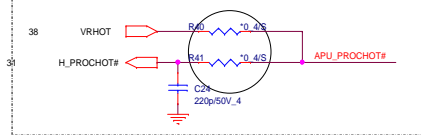
12/21 change to shortpad

APU Serial VID

Place near APU within 500mil
CRB: SVC & SVD 22 ohm follow check list 0 ohm.

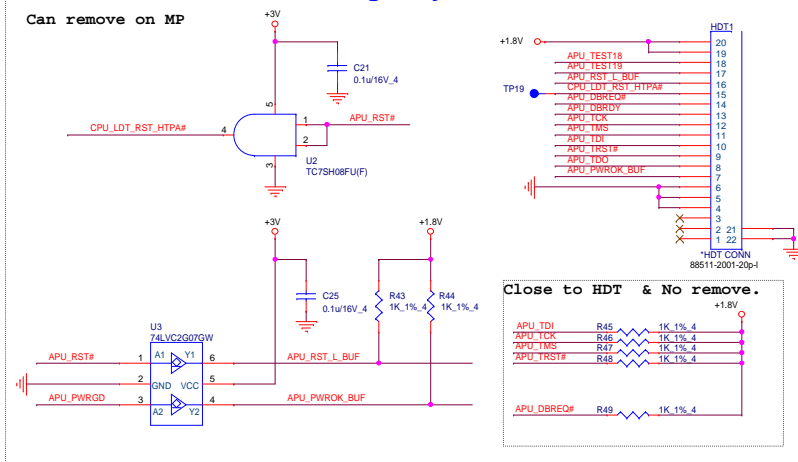
11/22 short pad

EC H_PROCHOT#

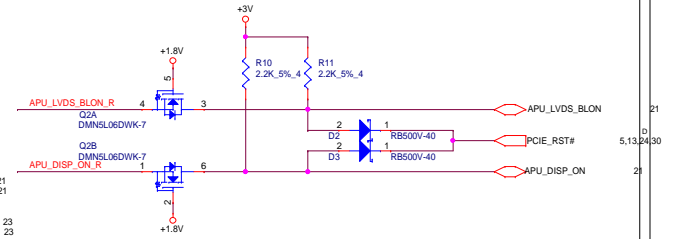


HDT+ Connector for Debug only

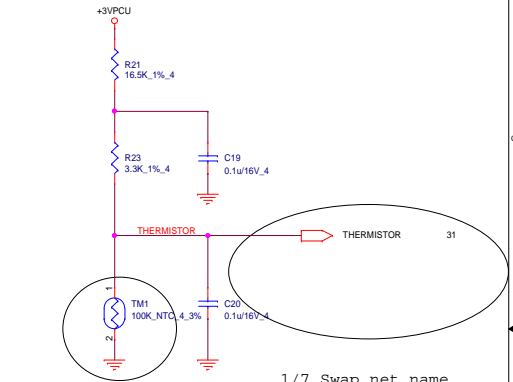
Can remove on MP



Close to HDT & No remove.



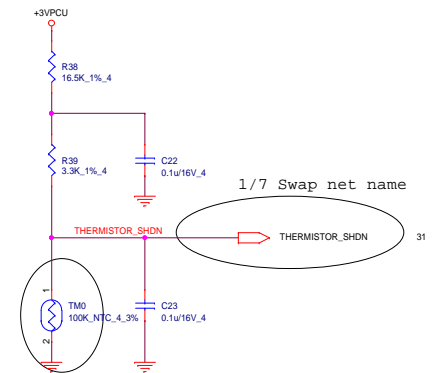
CPU Thermal Protect



1/7 Swap net name

01/04 change location name

Pipe Thermal Protect



1/7 Swap net name

01/04 change location name

BOARD ID SETTING

Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	1.4"
01	Reserve
10	Reserve
11	Reserve

Board ID [4:3]	Definition
00	Reserve
01	Reserve
10	Reserve
11	Reserve

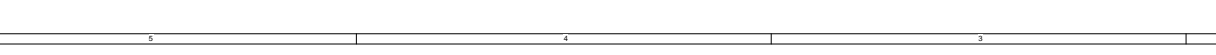
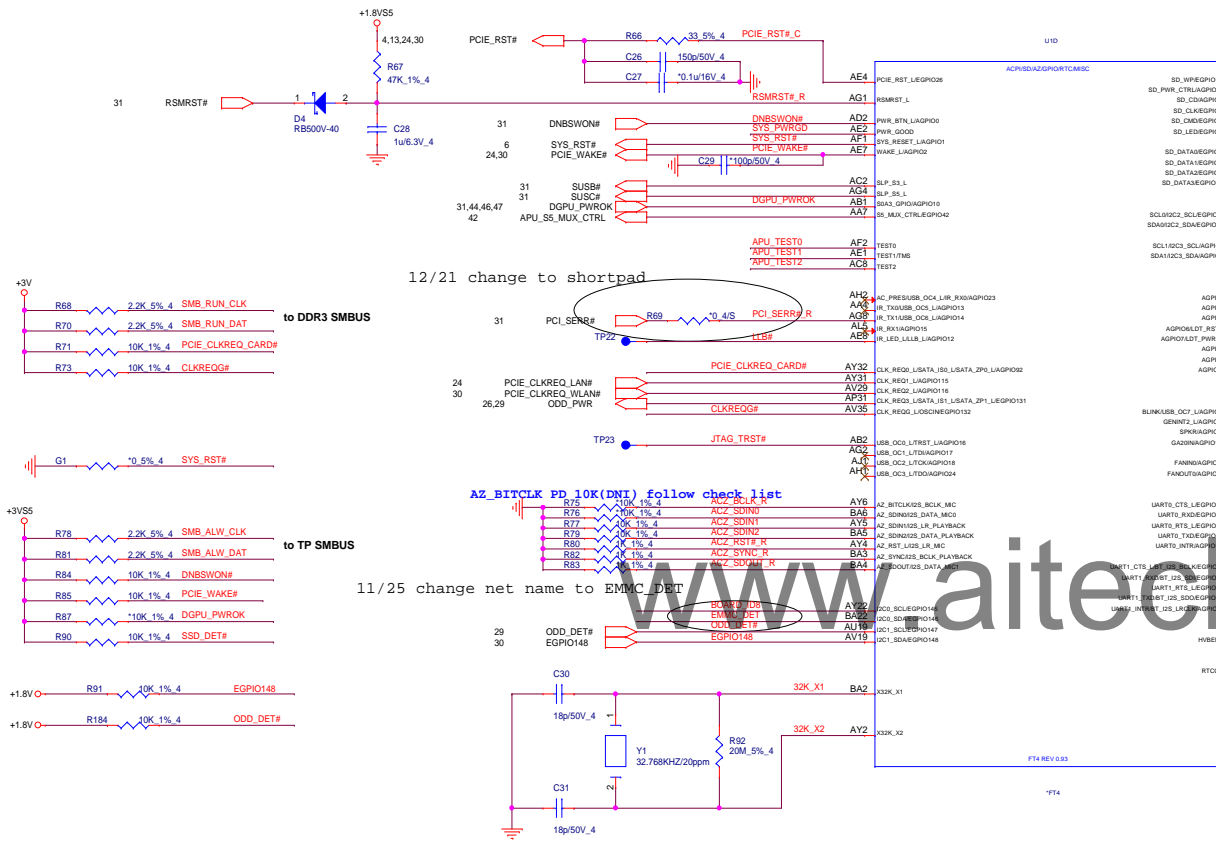
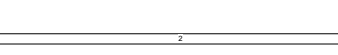
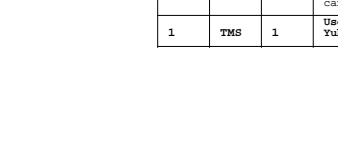
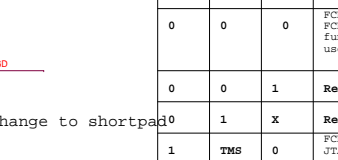
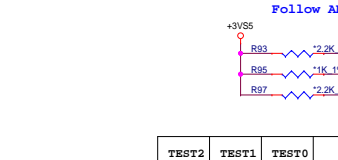
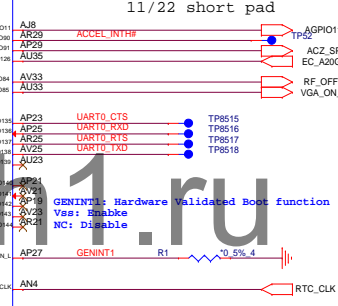
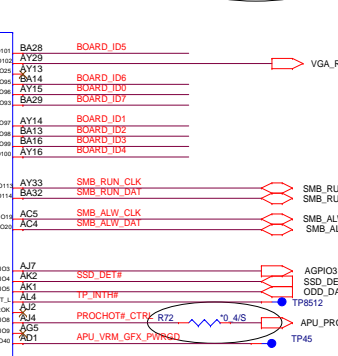
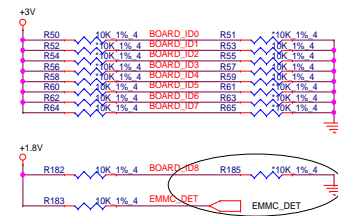
Board ID [5]	Definition
0	BR
1	SR

Board ID [6]	Definition
0	VRAM x8
1	VRAM x4

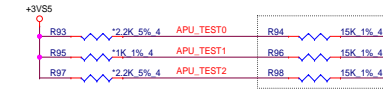
Board ID [7]	Definition
0	R17M-M1-70
1	R17M-M1-30

Board ID [8]	Definition
0	6W CPU
1	15W CPU

12/21 add CPU Watt.



Follow AMD checklist 55347 suggestion.



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled

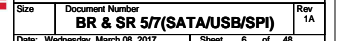


PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

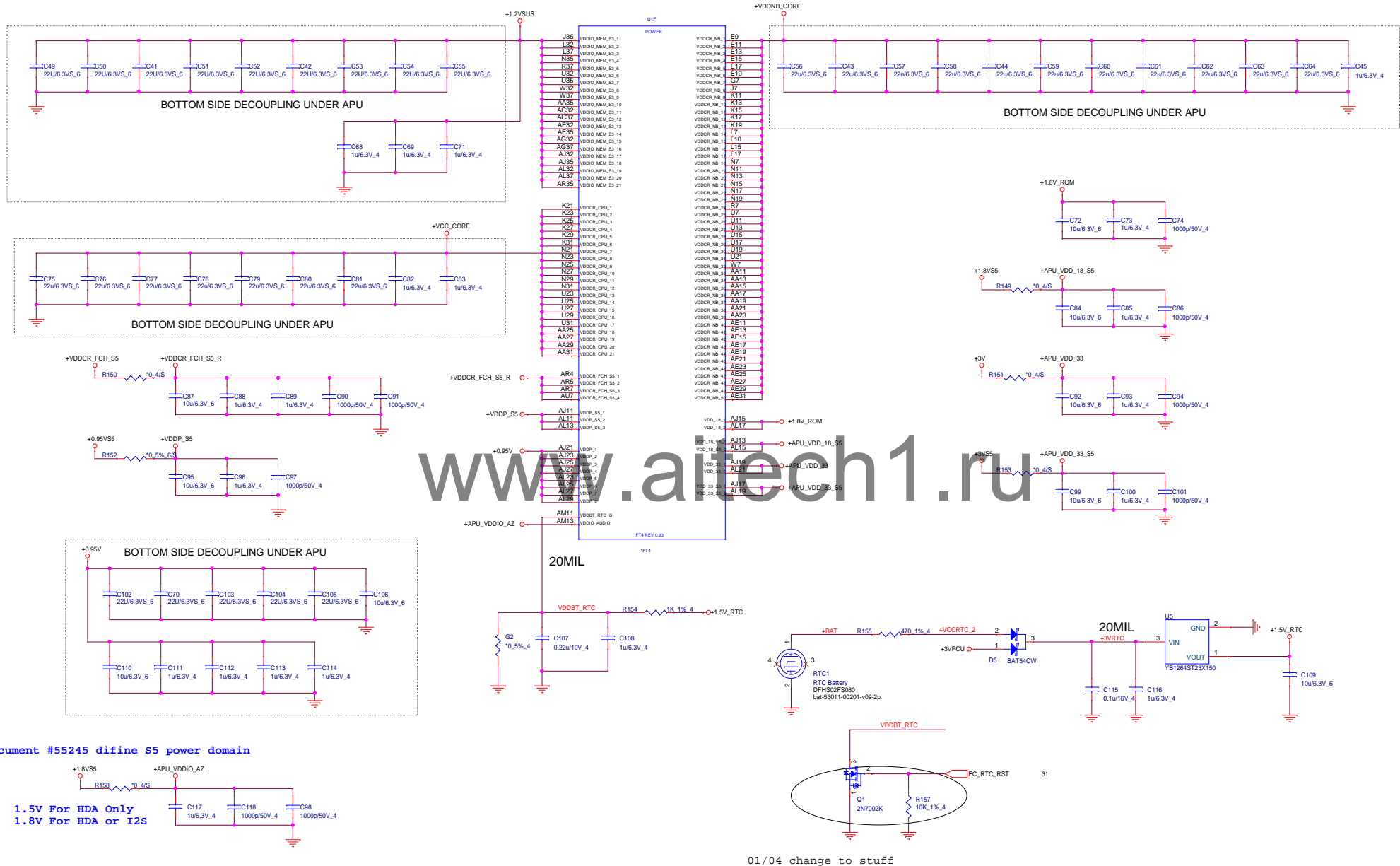
Size: Document Number: **BR & SR 47(GPIO/AZ/UART)** Rev 1A
Date: Wednesday, March 08, 2017 Sheet 5 of 48



For EMI
APU_SPI_CLK
EC3
*10p/50V 4

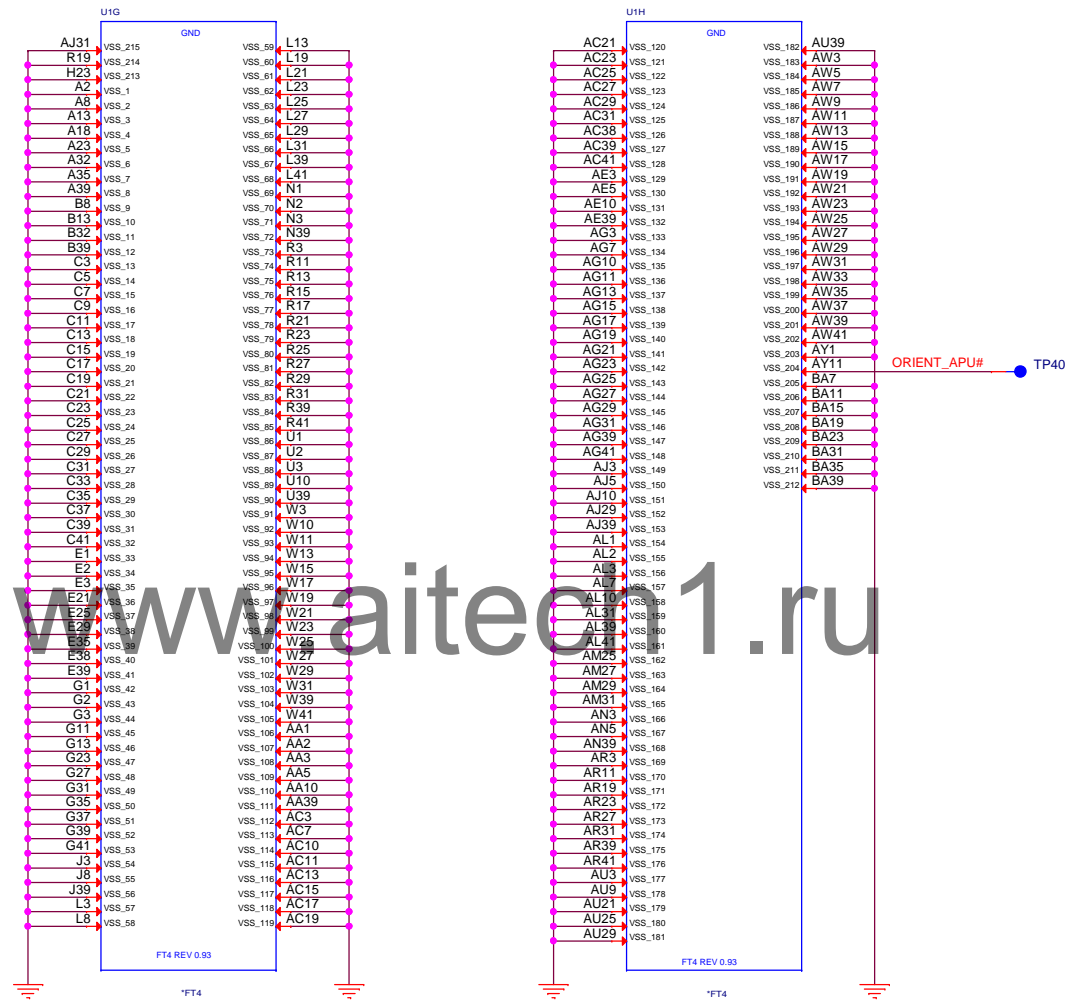


Power Decoupling follow Check list by AMD suggestion



AMD document #55245 define S5 power domain


01/04 change to stuff

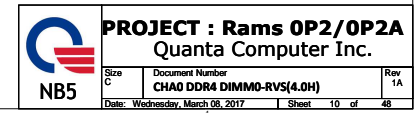
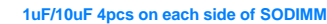


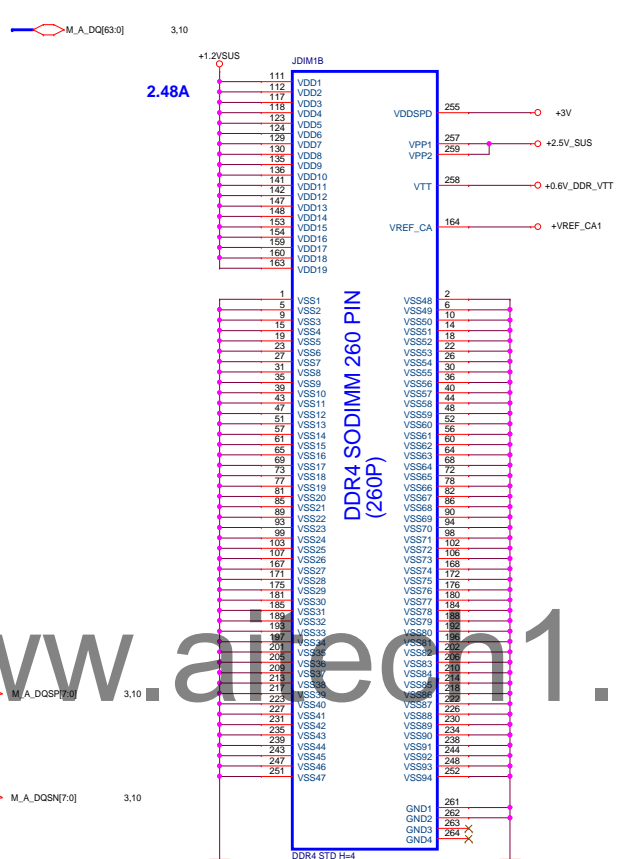
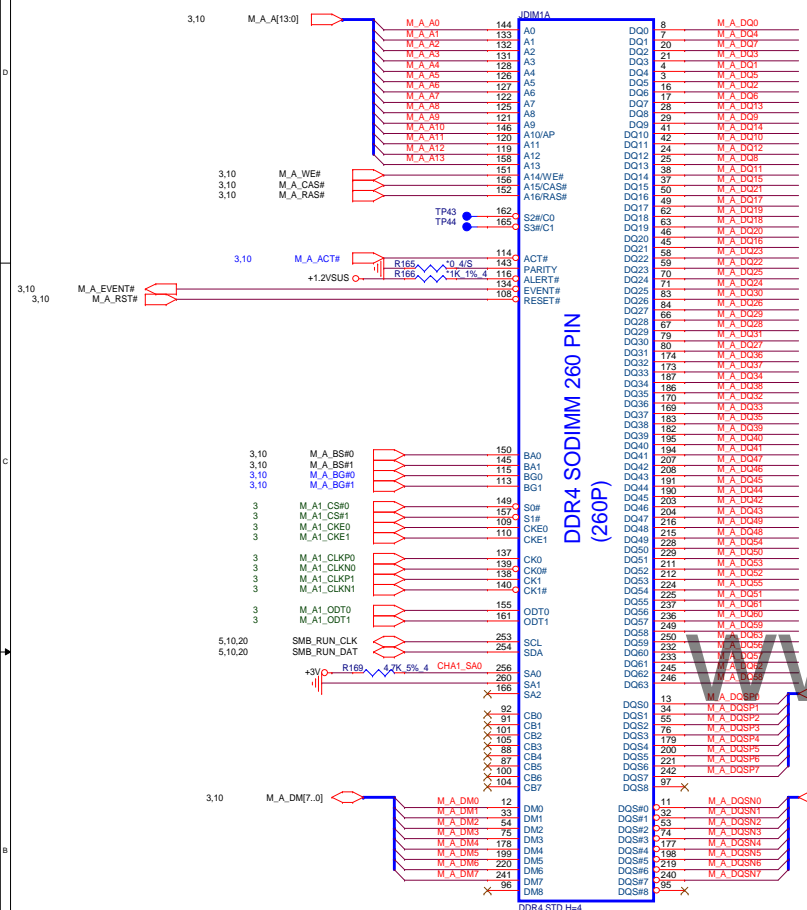
PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

Size	Document Number	Rev
	ST 717 (GND)	1A
Date: Wednesday, March 08, 2017 Sheet 8 of 48		

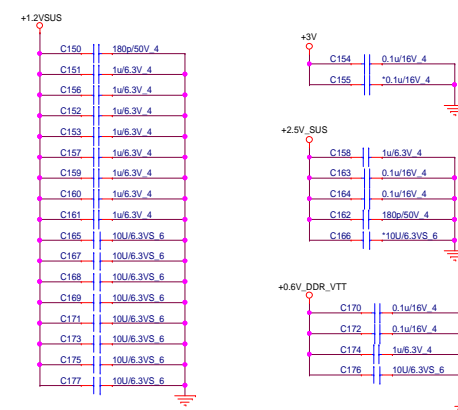
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 NB5	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Wednesday, March 08, 2017 Sheet 9 of 48		





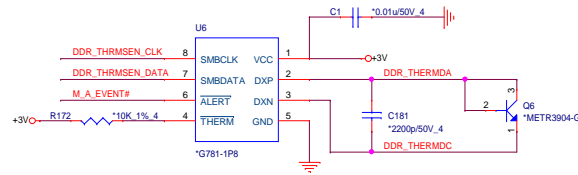
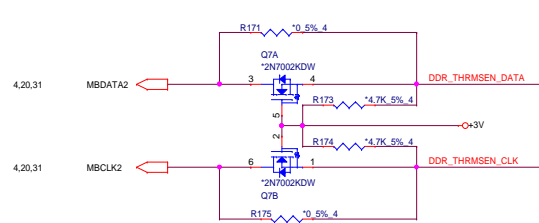
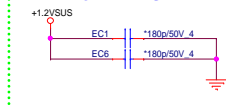
Place these Caps near SODIMM



1uF/10uF 4pcs on each side of SODIMM




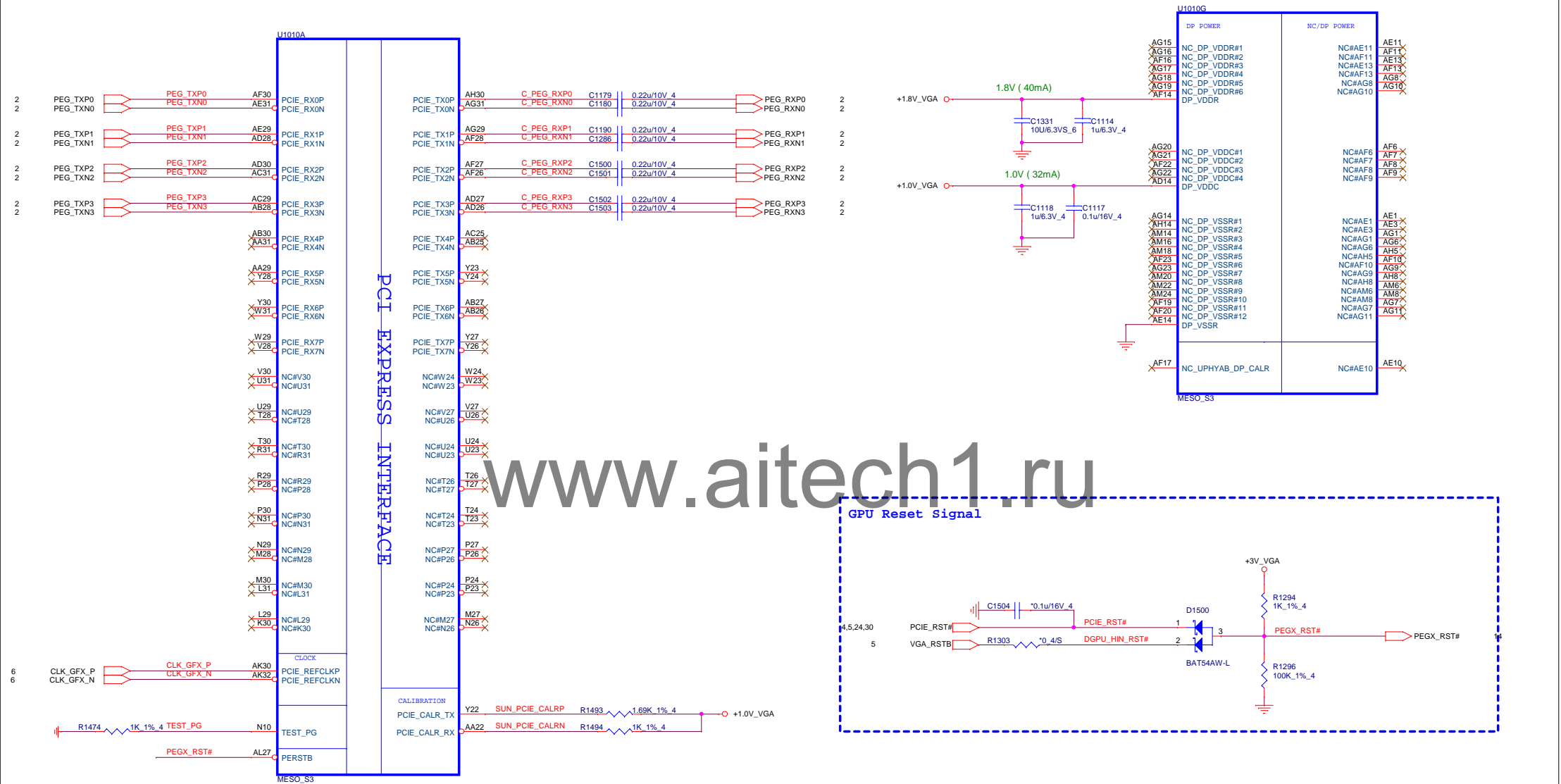
For EMI CAP

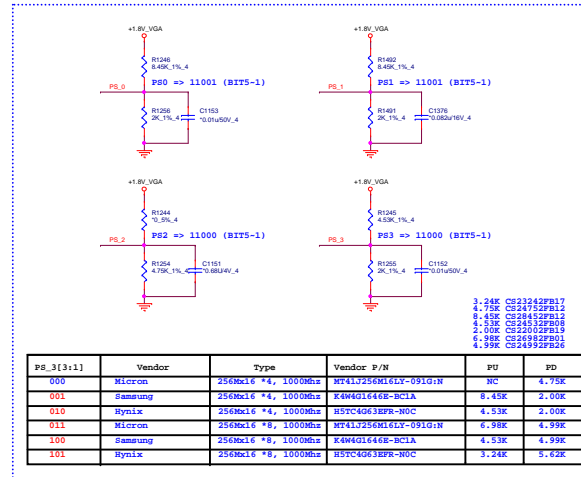


Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

<Reserved>
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 NB5	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Wednesday, March 08, 2017 Sheet 12 of 48		

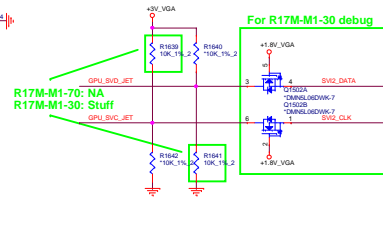


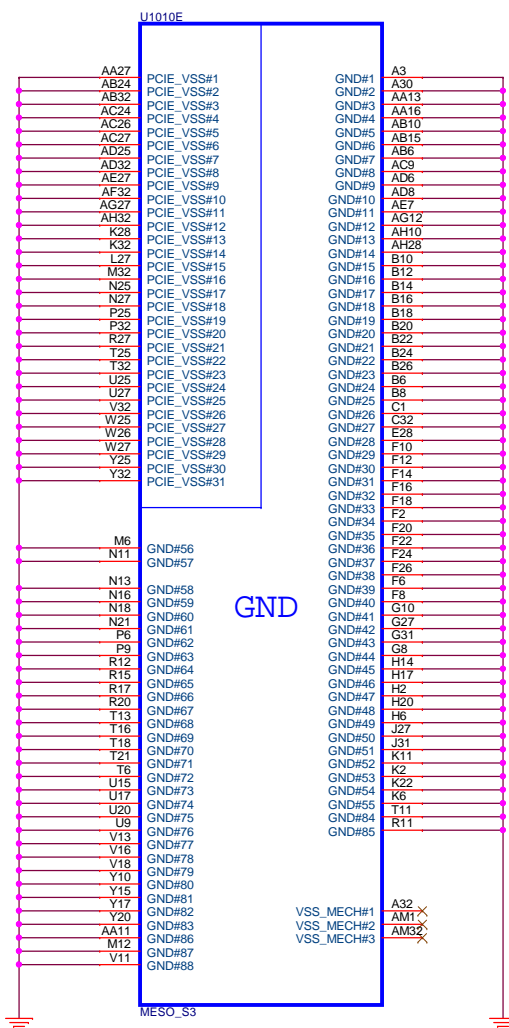


R _{pu} (Ohm)	R _{pd} (Ohm)
NC	4750
8450	2000
4530	2000
6980	4990
4530	4990
3240	5620
3400	10000
4750	NC

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

ALPNs URI	Strap Name	Description	Recommended Settings
PS_0101	ROM_CONFIG01	If STRAP_ROM_EN = 1, ROM_CONFIG01 defines the ROM type.	Design dependent, see the description.
PS_0102	ROM_CONFIG11	If STRAP_ROM_EN = 0, ROM_CONFIG11 defines the primary memory access type. See Security Memory Access Type (p. 29).	Design dependent, see the description.
PS_0103	ROM_CONFIG21	Reserved for internal use only.	0
PS_0104	N/A	Must be 1 at reset.	1
PS_0105	N/A	Reserved.	0
PS_0106	STRAP_SF_CGEN3_EN_A	PCIE GEN3 capability. 0 = PCIE GEN3 is supported. 0 = PCIE GEN3 is not supported.	Design dependent, see the description.
PS_1101	STRAP_BIF_CLK_PN_EN	Continue operation or not the PCIe reference clock power management capability is reported in the PCIe configuration space (clockpower in CTR040).	0
PS_1102		0 = The CLEURREF power management capability is disabled. 1 = The CLEURREF power management capability is enabled.	1
PS_1103	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1104	STRAP_TX_CPOV_BURN_PVLLI_EN	Control the transmitter full-voltage level. 0 = The transmitter full-voltage is enabled. 1 = The transmitter full-voltage is disabled.	1
PS_1105	STRAP_TX_DEENPH_EN	PCI EXPRESS® transmitter de-emphasis enable. 0 = Tx deemphans disabled. 1 = Tx deemphans enabled.	Design dependent, see the description.
PS_2101	N/A	Reserved.	0
PS_2102	N/A	Reserved.	0
PS_2103	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2104	N/A	Reserved.	1
PS_3101	BOARD_CONFIG00	Reserved.	0
PS_3102	BOARD_CONFIG01	Board configurations related strapnames such as for memory ID.	Design dependent, see the description.
PS_3103	BOARD_CONFIG02	Reserved.	0
PS_3104	N/A	Reserved.	0
PS_3105	N/A	Reserved.	0





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS **ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,** **THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

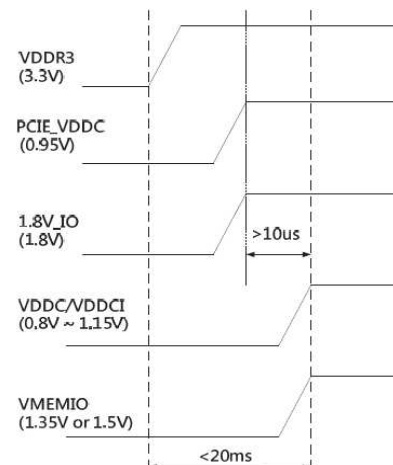
NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

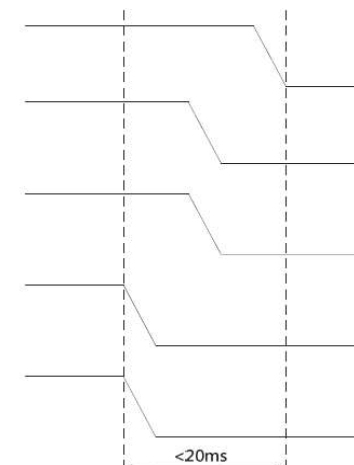
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

POWER UP

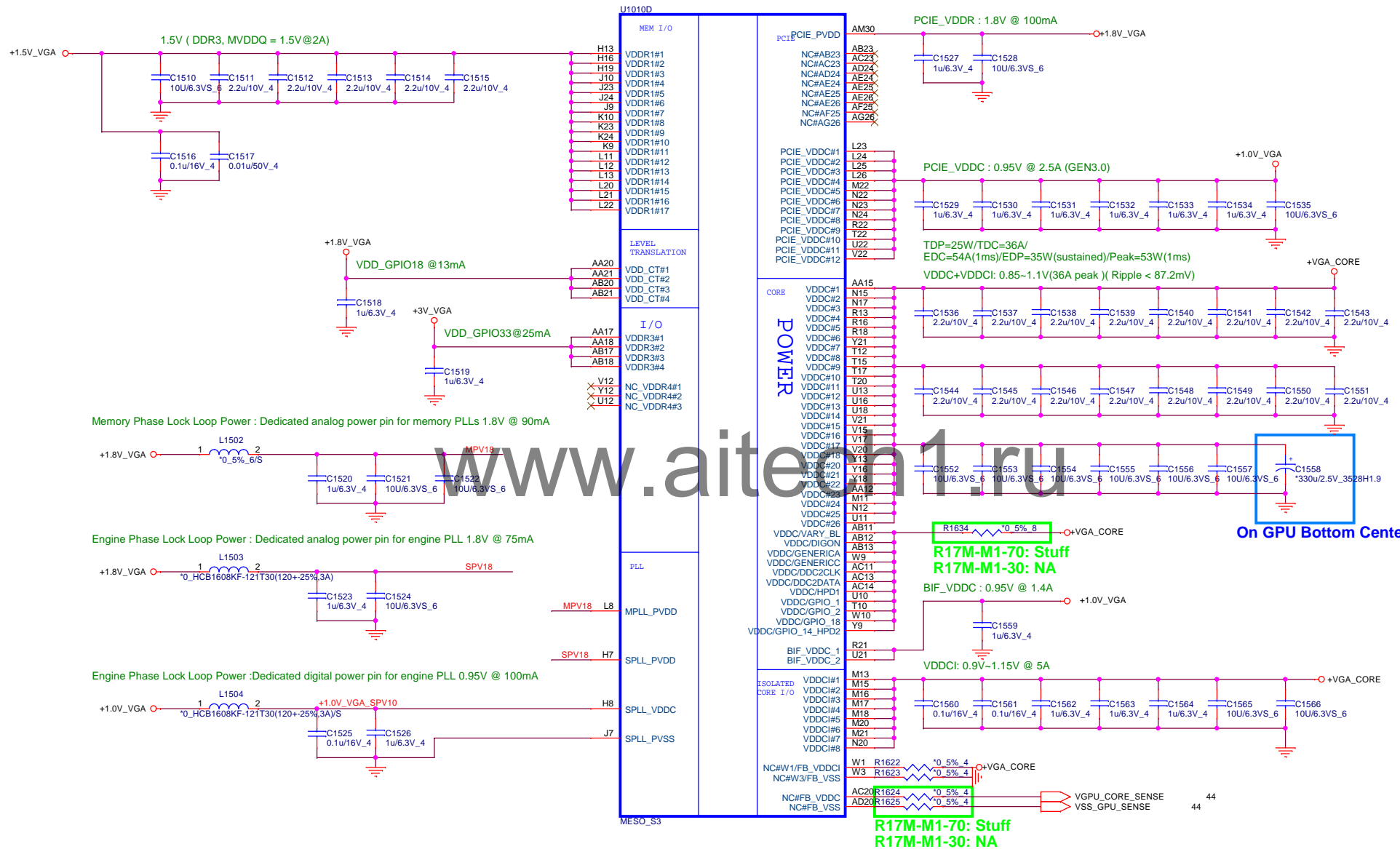


POWER DOWN



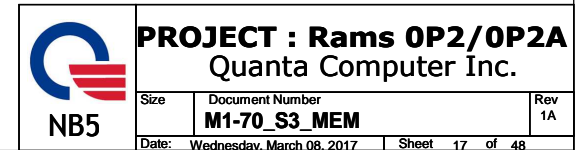
PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

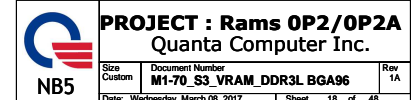
Size	Document Number	Rev
	M1-70_S3_GND/LVDS/Strap	1A
Date:	Wednesday, March 08, 2017	Sheet 15 of 48



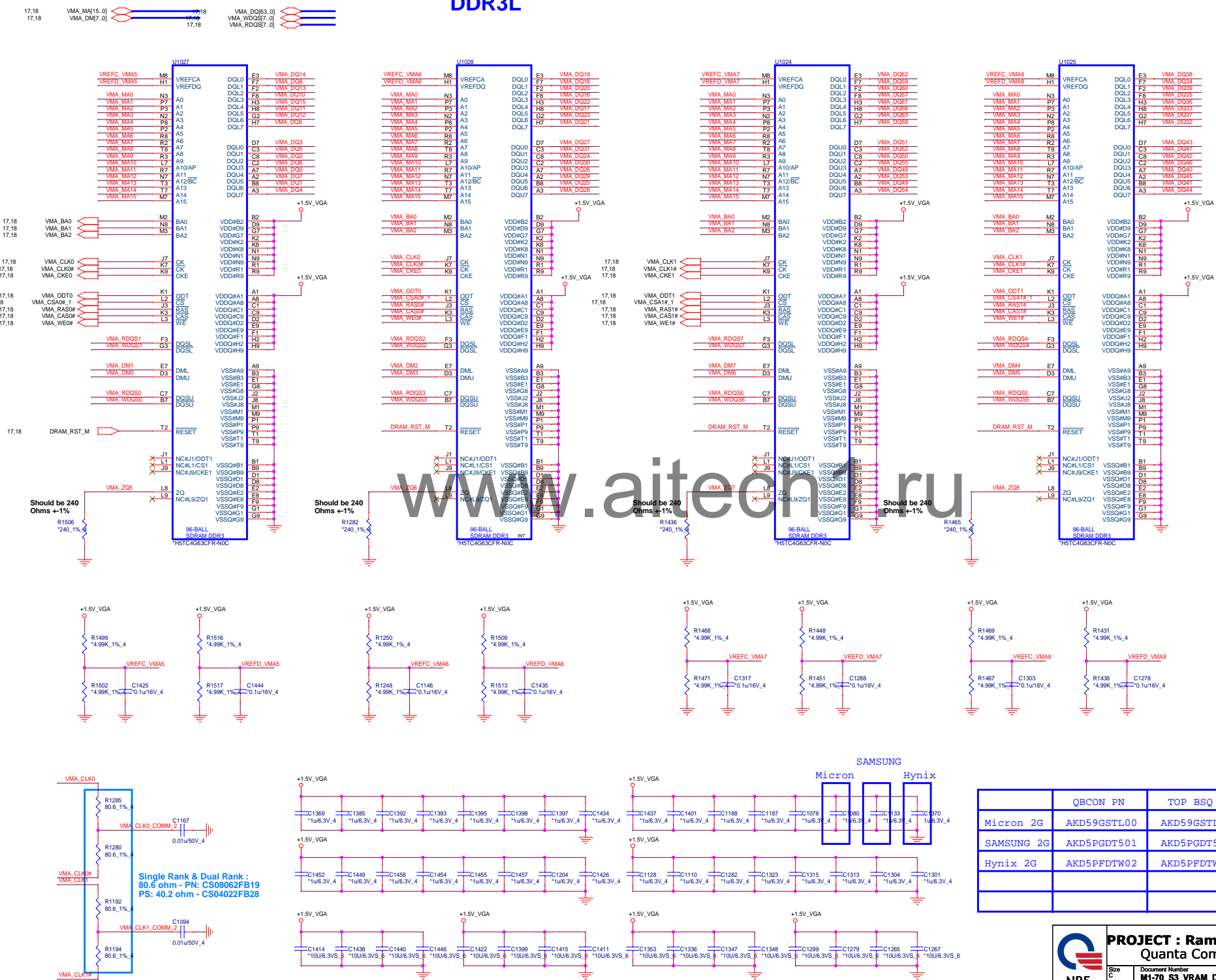
PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3 POWER	1A
Date:	Wednesday, March 08, 2017	Sheet 16 of 48

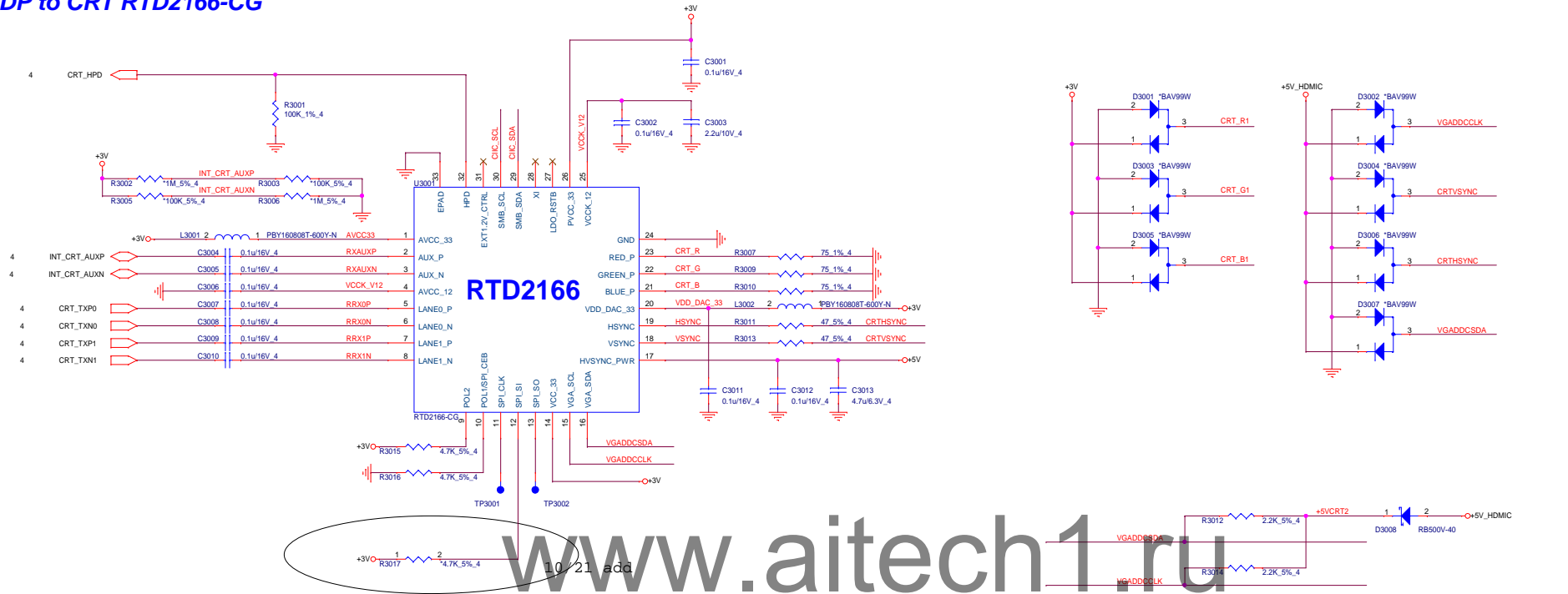




DDR3L



DP to CRT RTD2166-CG



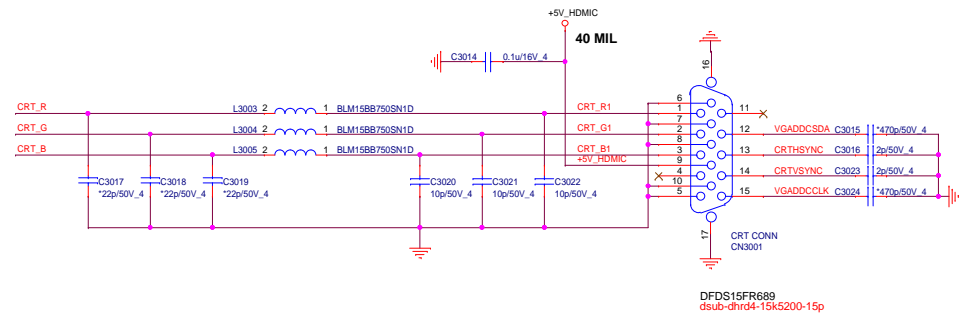
CIIC_SCL, CIIC_SDA Connection

EP mode: Pin2, Pin3 connect to EC SMBUS
 ROM or EEPROM mode: connect to PCH SMBUS
 IIC Protocol is used

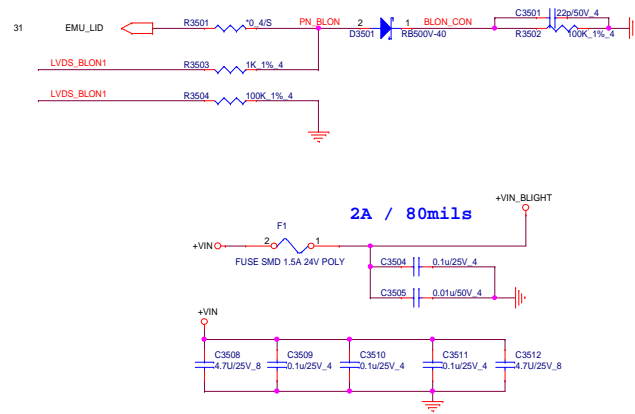
From PCH



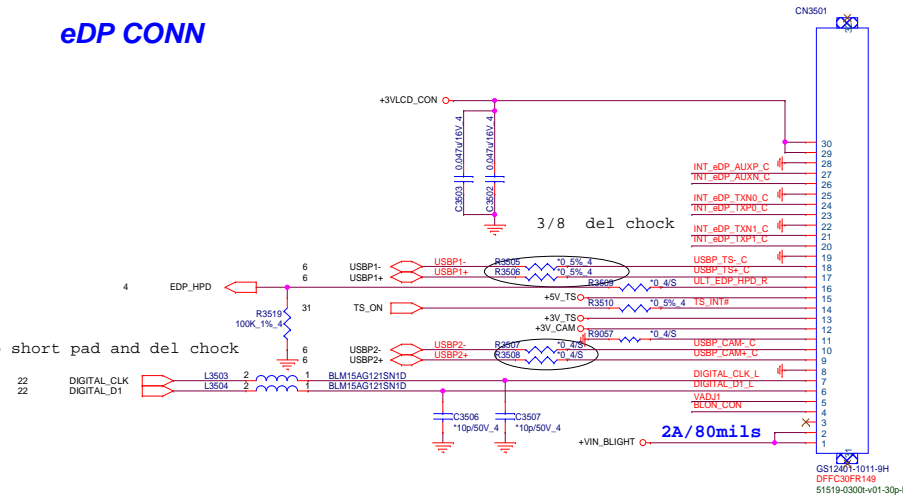
From EC



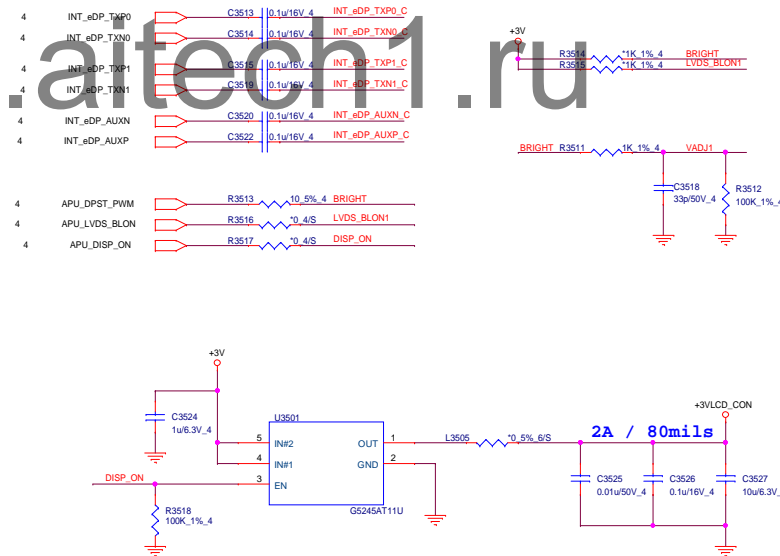
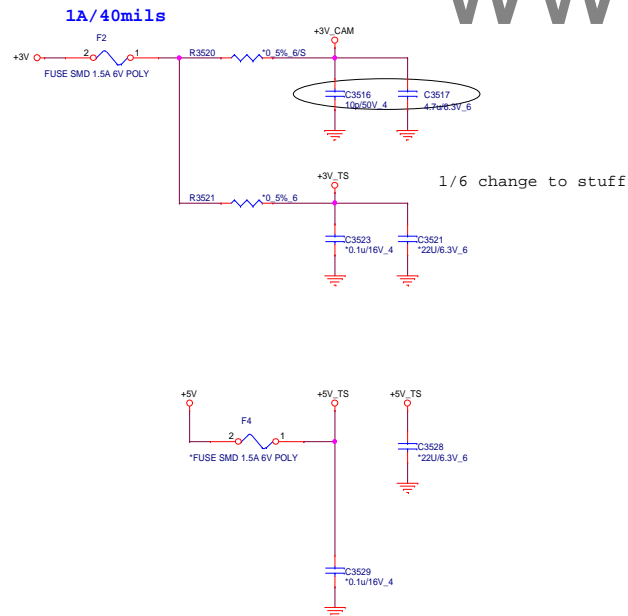
LID Switch

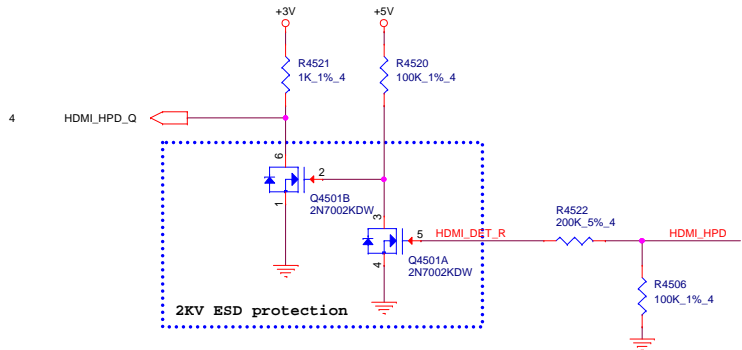
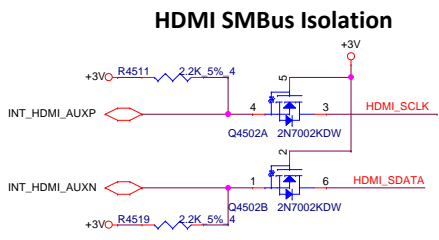
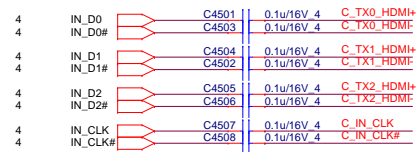


eDP CONN

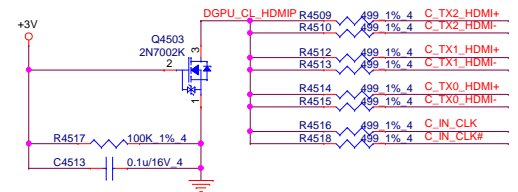


Touch screen

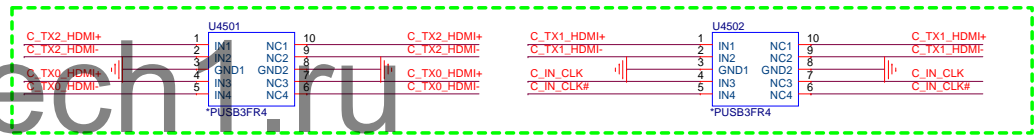
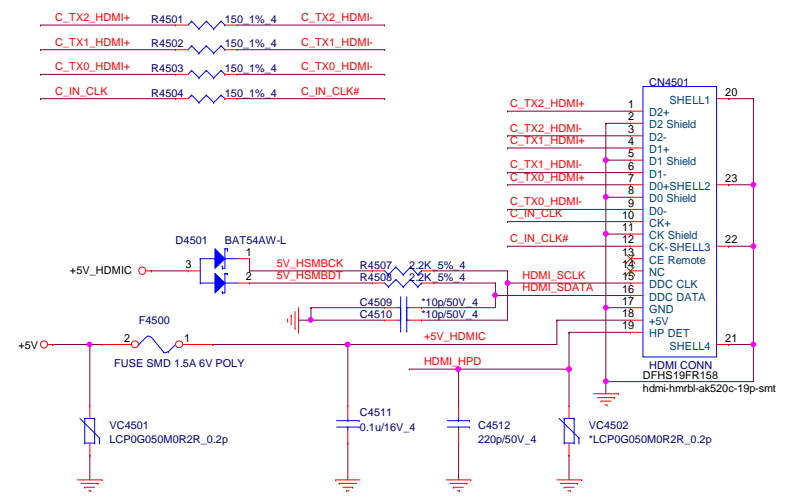




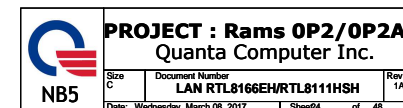
Close to HDMI connector

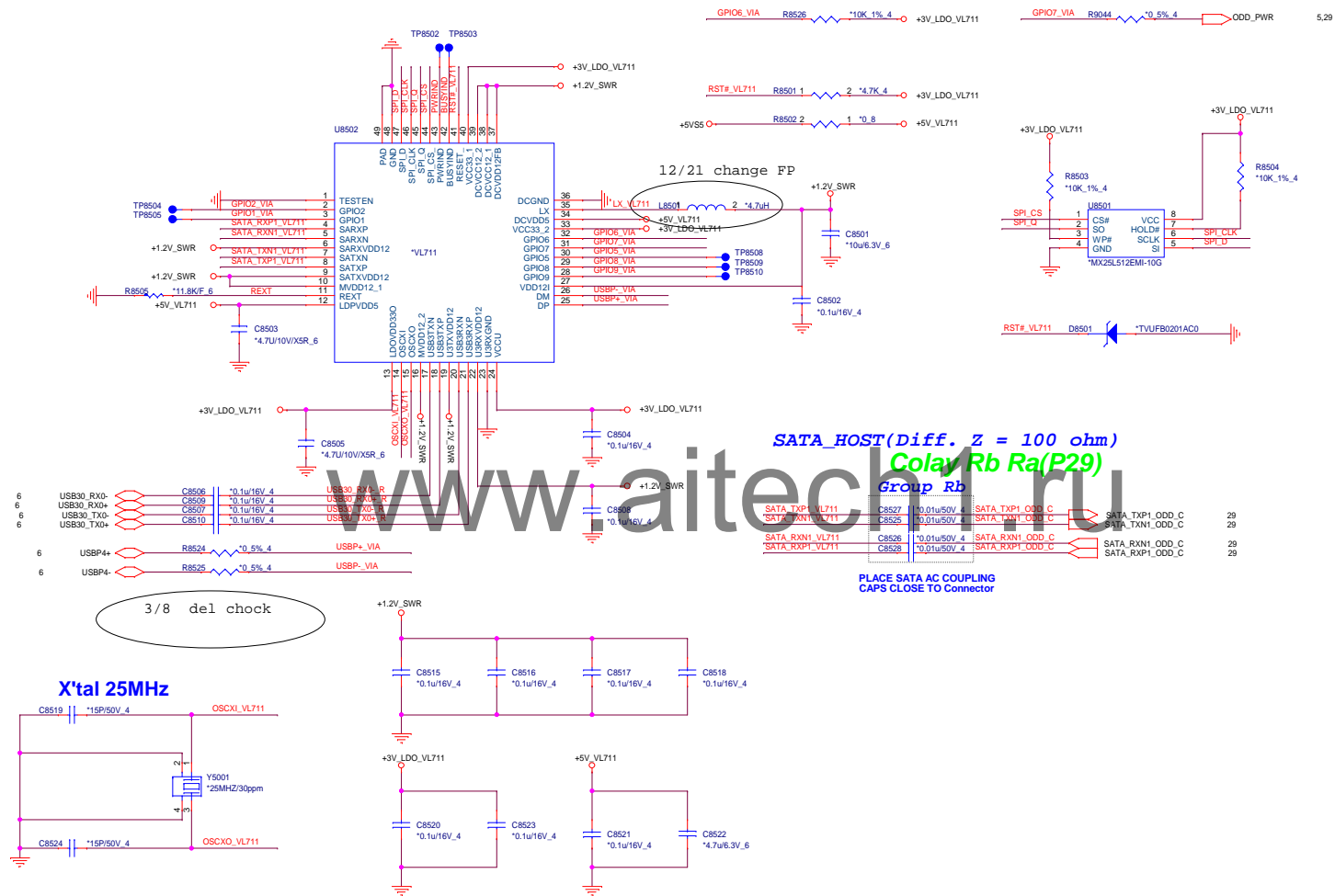


EMI Solution

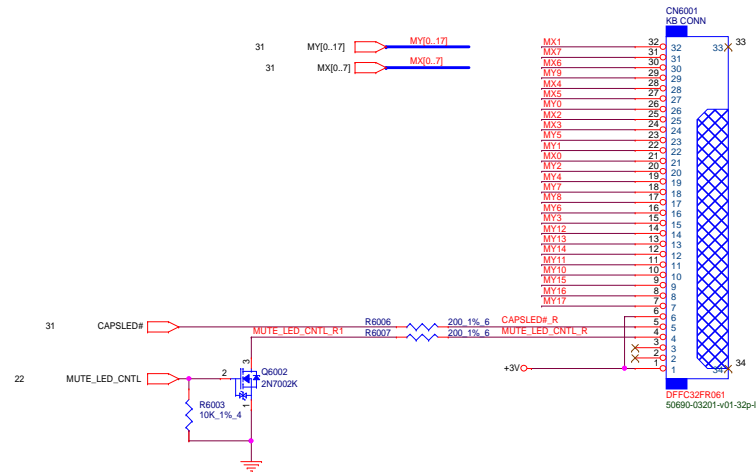


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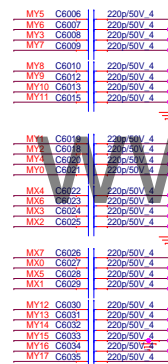
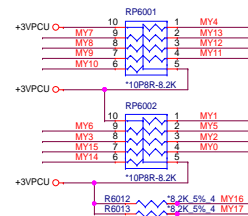




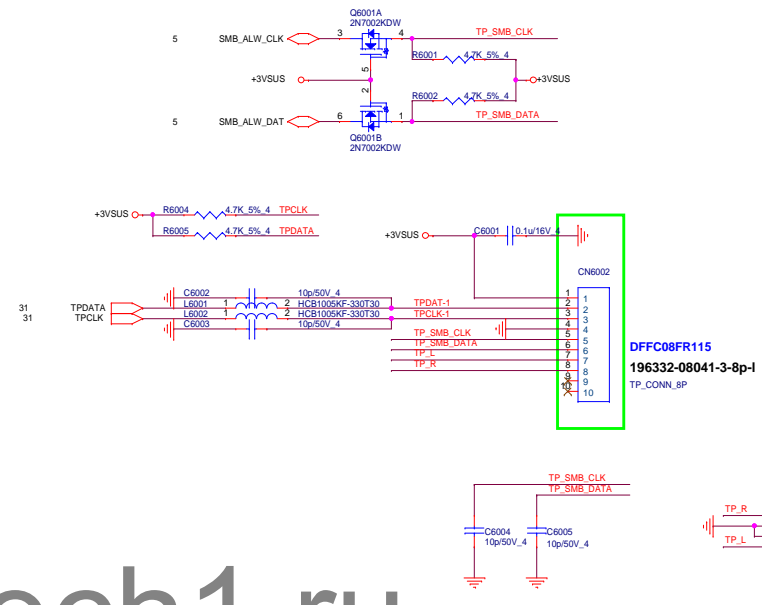
KEYBOARD CONN



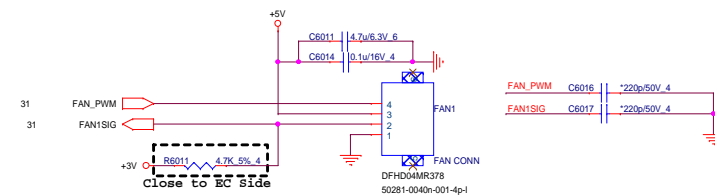
KEYBOARD PULL-UP



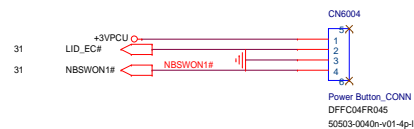
Touch Pad CONN



FAN CONN

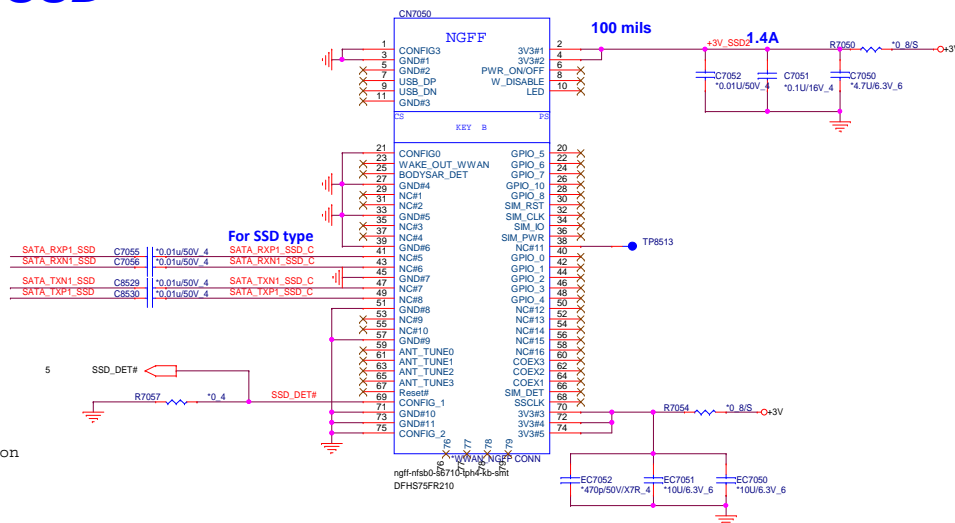


Power Button



2nd SATA SSD

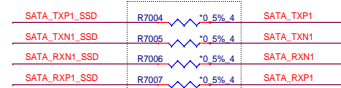
29



10/20 add 2nd SSD function

Group Rb

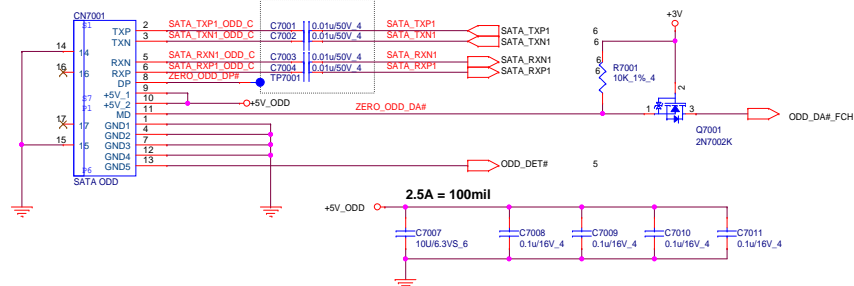
Close ODD side, Colay Top / Bot side for branch!!



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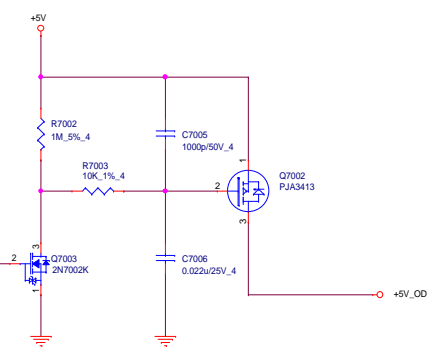
SATA ODD Colay Ra Rb(P26)

Group Ra

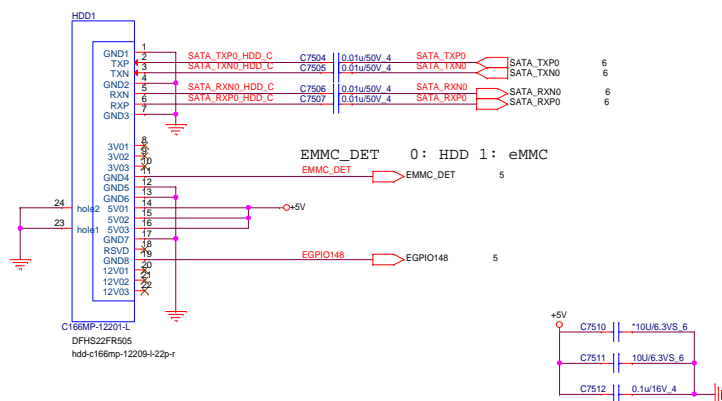


High : ODD power on
Low : ODD power down

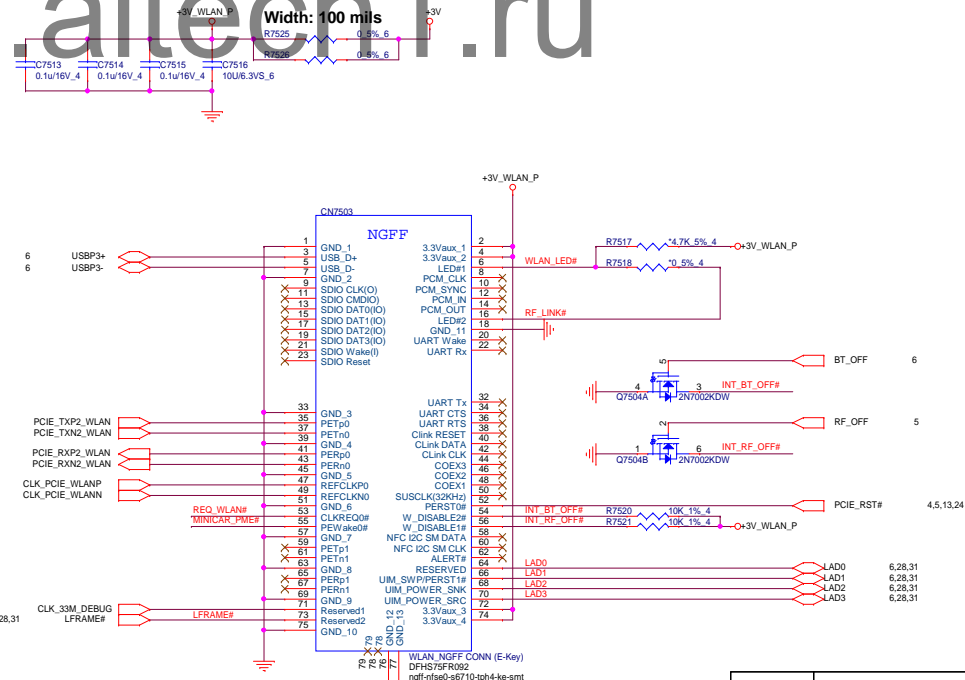
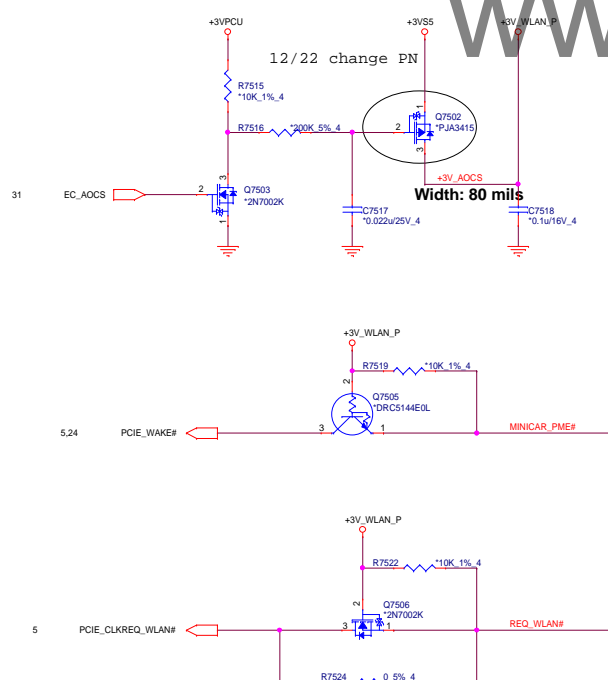
5.26 ODD_PWR

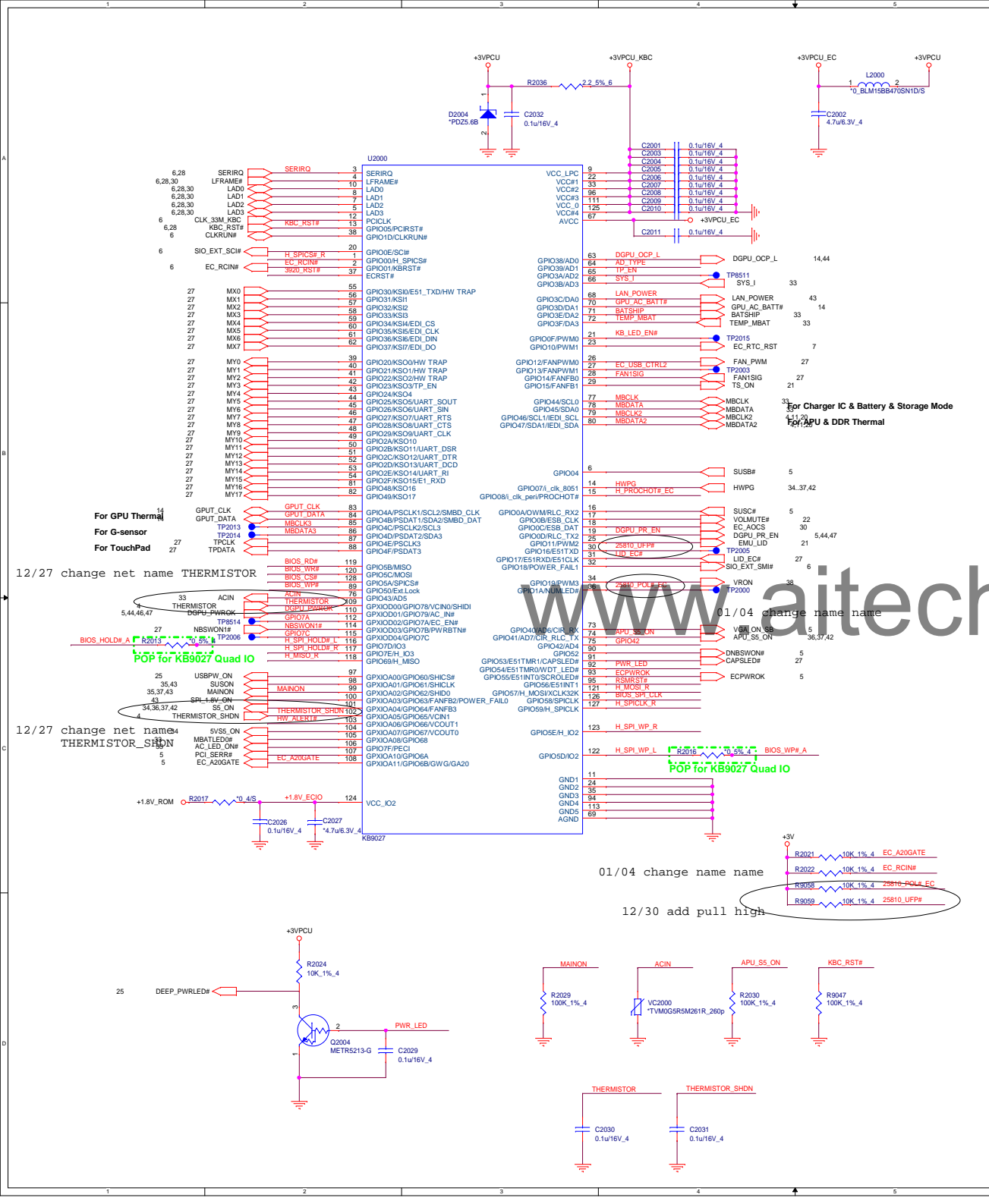


SATA HDD

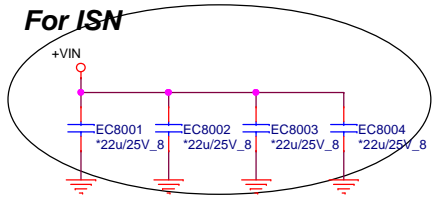


WLAN & BT

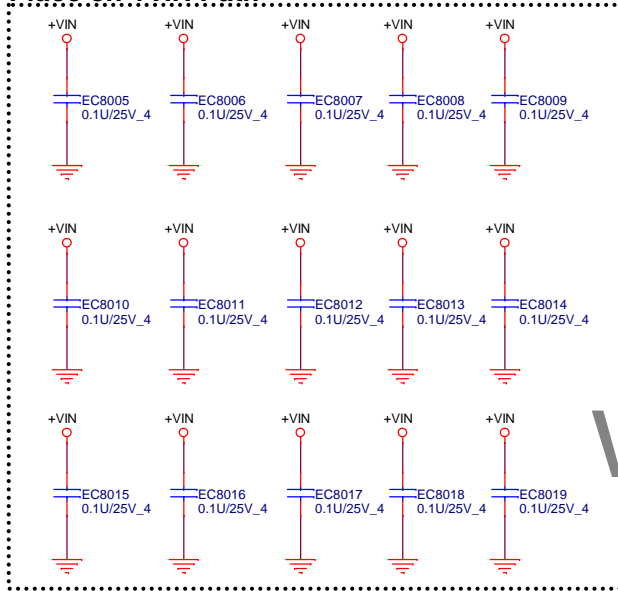
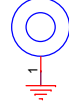
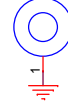
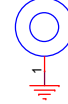
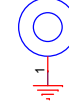
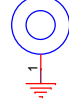
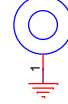
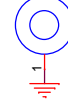
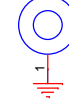
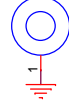
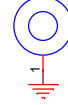
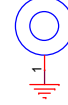
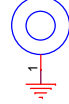
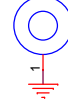
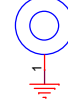
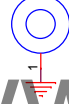
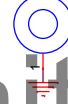
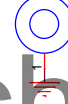




For ISN



Place on +VIN Path

H1
*H-C237D130P2H25
*H-OP1-1H29
*PAD-BALL276-NPH34
*PAD8_0X1_5MM-NPH26
*H-TBC276IC158D118P2H27
*H-CT315B400SI178D158P2H28
*PAD-BALL276-NPH33
*PAD13_65X3_5MM-NPH2
*H-TBC276IC198D158P2H3
*H-OP2-1H30
*H-IC276BC315D154PBH24
*H-TBC315IC158D118P2H8
*H-OP2-1H31
*H-IC276BC315D154PBH7
*H-OP1-1H4
*H-OP2-1H32
*H-OP2-1

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**PROJECT : Rams 0P2/0P2A**
Quanta Computer Inc.

Size	Document Number	Rev
B	EMI CAP/HOLES	1A

Date: Wednesday, March 08, 2017 Sheet 32 of 48

**Do Not add test pad on
BQBATDRV/BATDIS_ID_DOD signal**

Place this ZVS close to Diode away +VIN

$I_{dss} < 5\mu A$

Place this ZVS close to
Far-Far away +VIN

Place this cap
close to EC


Timing diagram for the BQ4Z728HRGRR device. The diagram shows various signals over time, including BQACDRV, ACDRV, BTST, PHASE, BOPHASE, BQLODRV, and ACIN. Key parameters like PR20, JQK, and PC22 are indicated. The diagram is overlaid with a large 'www.aitech.ru' watermark.

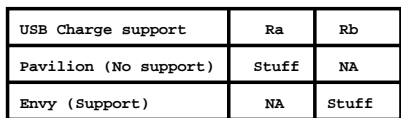
Place this cap
close to EC


Set MAX charge I to 5A

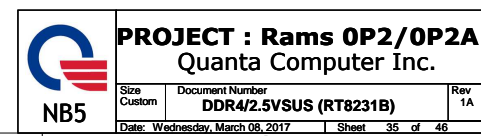
ACDET=13V

MIN. BATV=7.2V

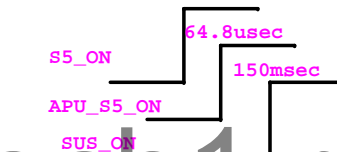
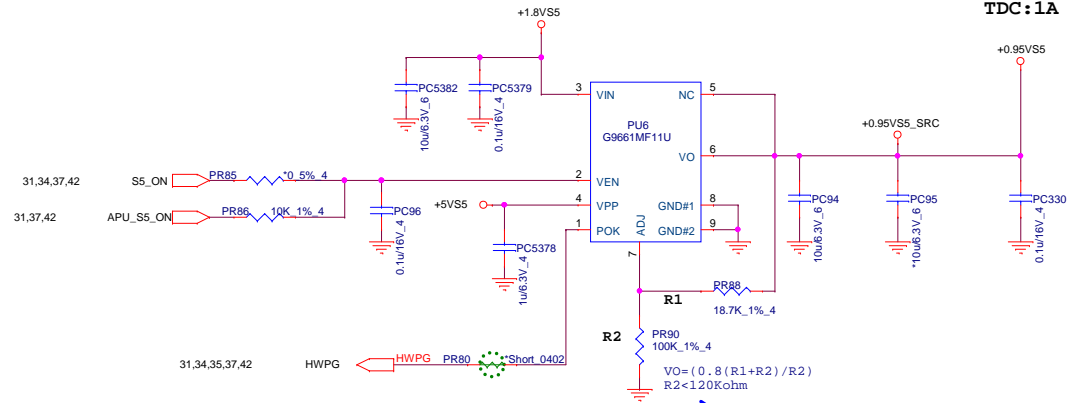
	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size Custom	Document Number Charger (BQ24728H)	Rev 1A
Date: Wednesday, March 08, 2017		Sheet 33 of 46	



	PROJECT : Rams 0P2/0P2A Quanta Computer Inc.		
	Size Custom	Document Number 3/5VSS (SY8286B/SY8286C)	Rev 1A
	Date: Wednesday, March 08, 2017	Sheet	34 of 46



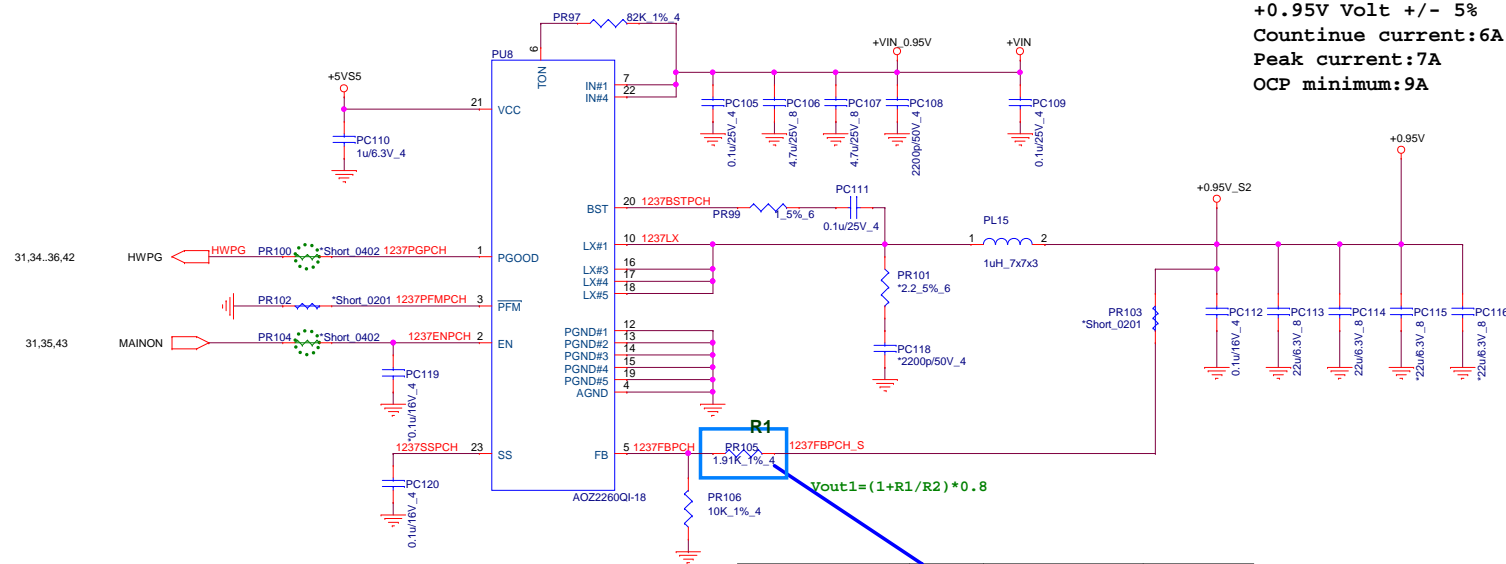
+0.95V +/- 5%
TDC:1A



	R1		
Stoney/Bristol	18.7K	CS31872FB19	0.95V
	31.6K	CS33162FB14	1.05V

Bristol VDDP=1.05V
Stoney VDDP=0.95V

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+0.95V Volt +/- 5%
Continue current:6A
Peak current:7A
OCP minimum:9A

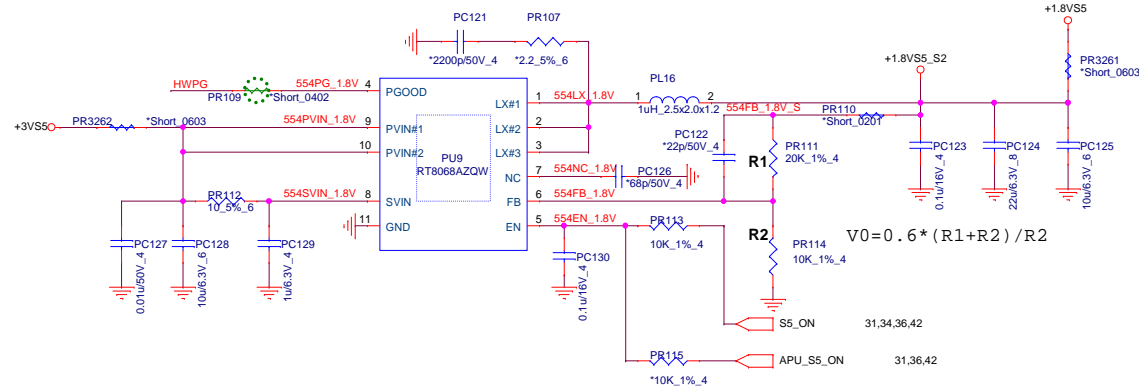
Bristol VDDP=0.95V
Stoney VDDP=0.95V

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

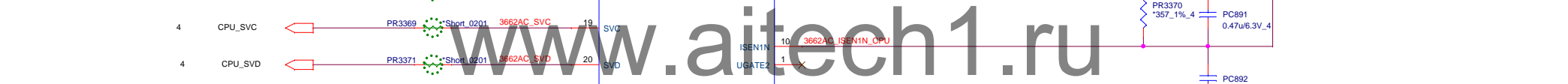
~~$$V_{out1} = (1 + R1/R2) * 0.8$$~~

	R1		
Stoney / Bristol	1.91K	CS21912FB13	0.95V
	3.16K	CS23162FB04	1.05V

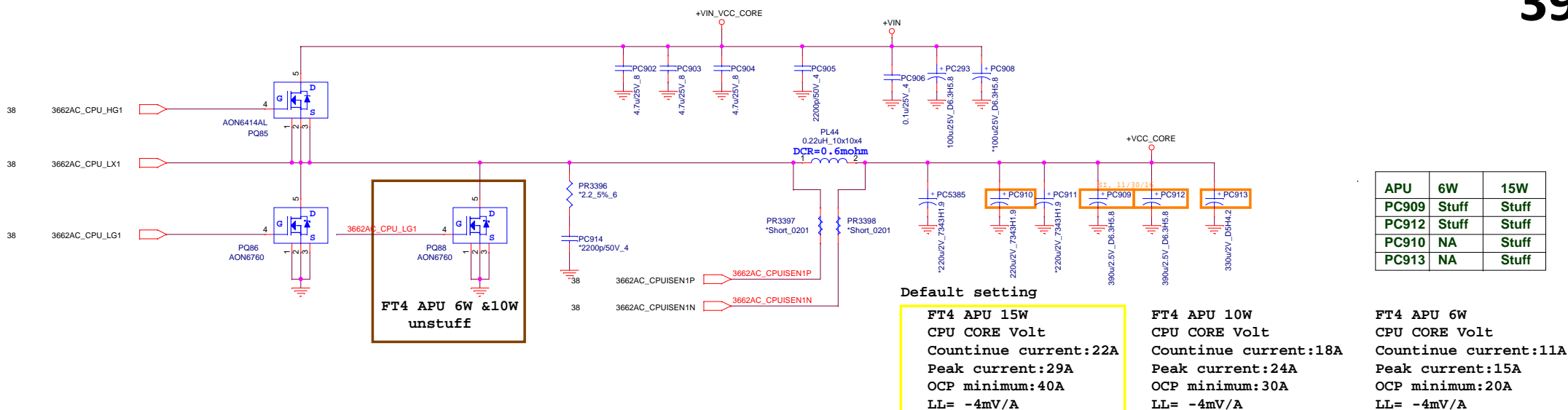
1.8VS5 +/- 3%
TDC:3A
EDP:4A



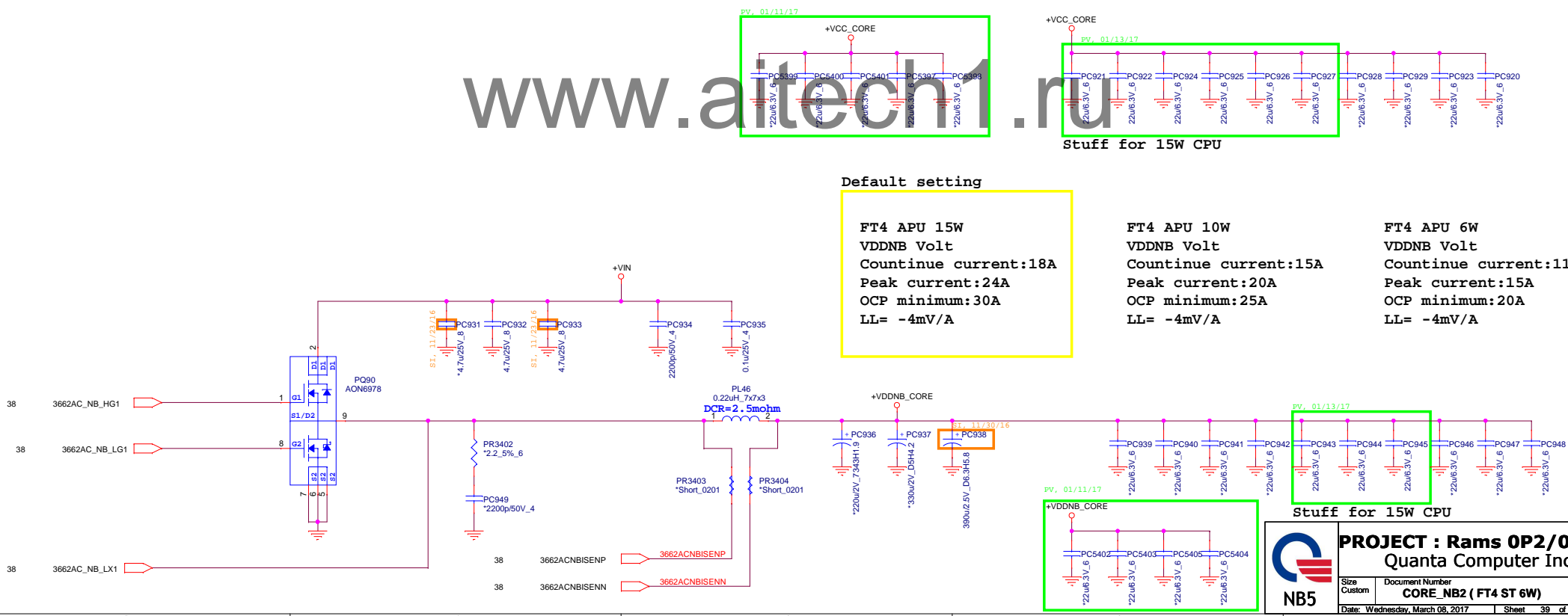
$$V_0 = 0.6 * (R_1 + R_2) / R_2$$




APU	6W	15W
Ra	16.9k	12.1k
Rb	13.3k	4.53k
Rc	9.31k	4.32k
Rd	15k	13k
Re	68.1k	34k
Rf	66.5k	42.2k



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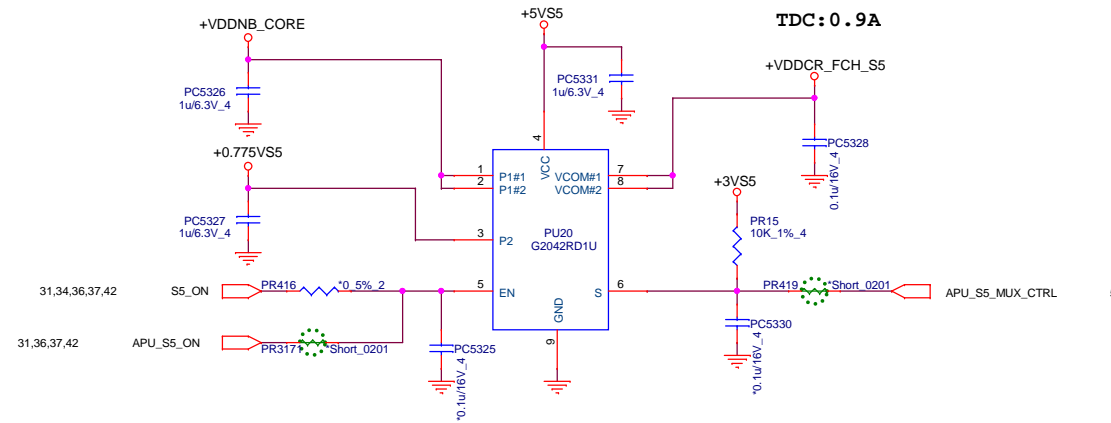


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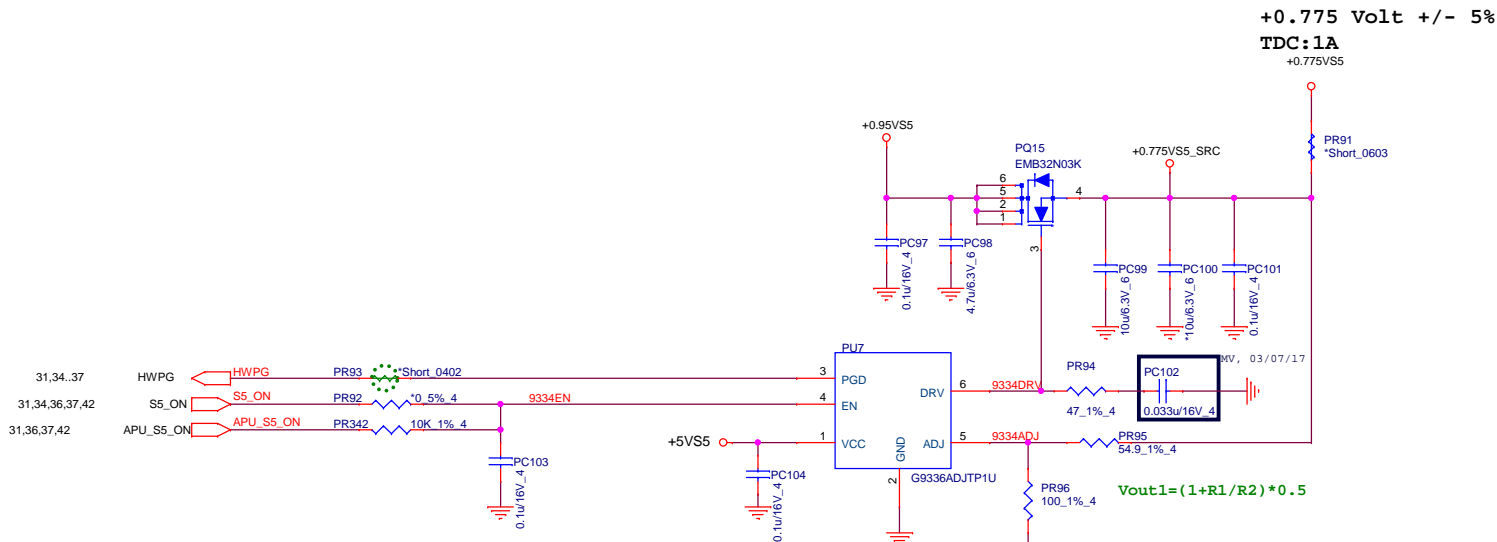
 NB5	PROJECT : Rams OP2/OP2A Quanta Computer Inc.			
	Size Custom	Document Number GFX1 (Stonlry N/A)		Rev 1A
	Date: Wednesday, March 08, 2017		Sheet	40 of 46

CPU	Page 40 & Page 41
Bristol	Stuff
Stonley FP4,FT4	Unstuff

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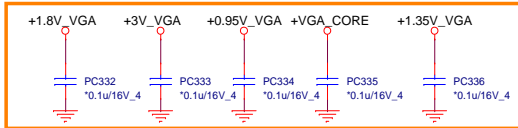


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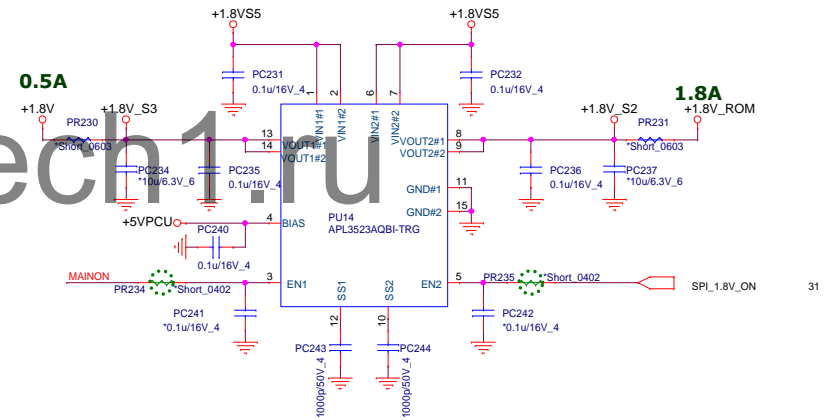
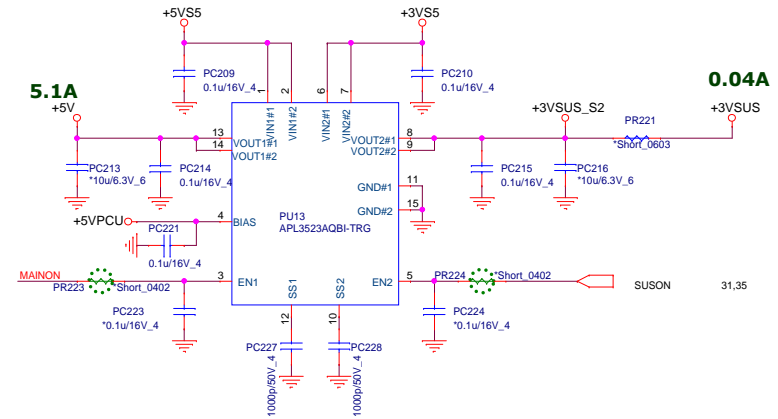
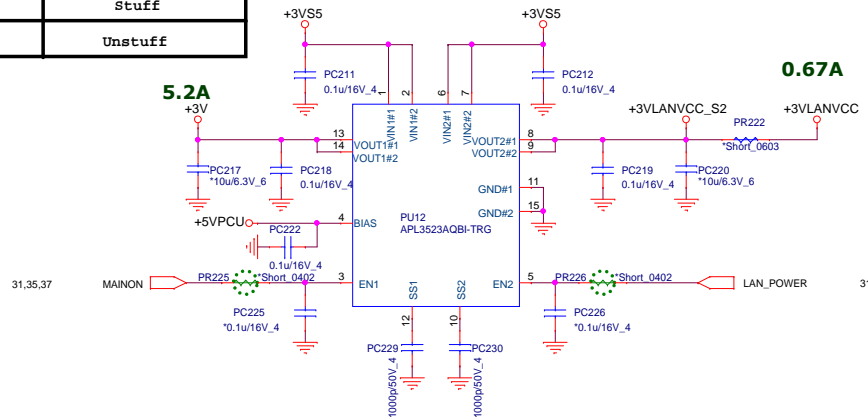


PROJECT : Rams OP2/OP2A
Quanta Computer Inc.

Size Custom	Document Number VDDCR_FCH/0.775VS5	Rev 1A
Date: Wednesday, March 08, 2017		



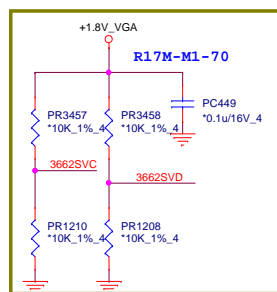
UMA only	Stuff
discrete	Unstuff



PROJECT : Rams 0P2/0P2A
Quanta Computer Inc.

Size Custom Document Number Load switch IC (APL3523A) Rev 1A

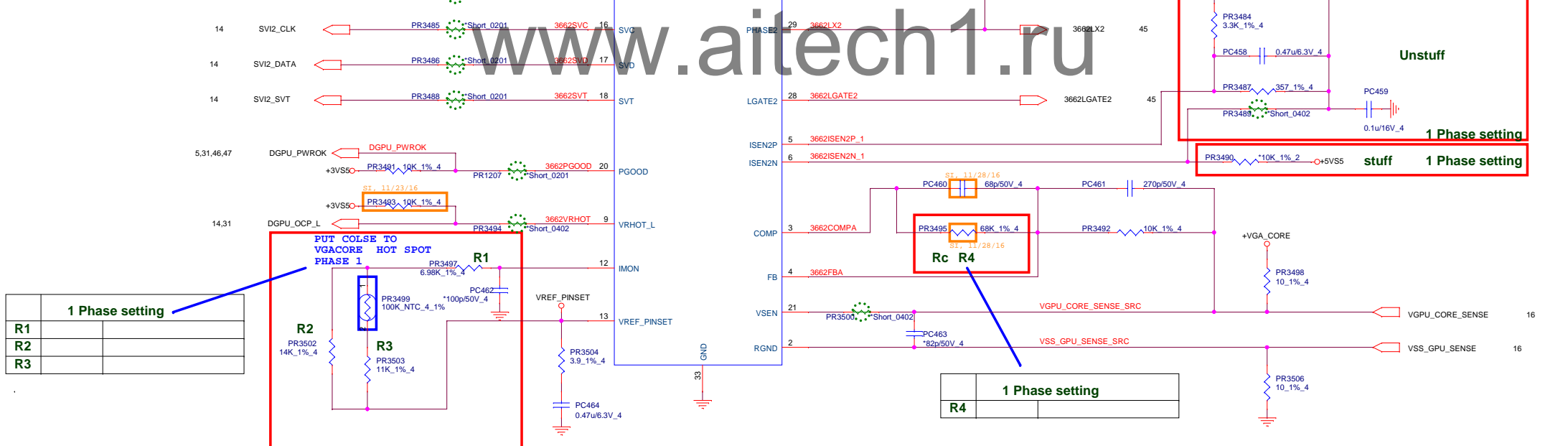
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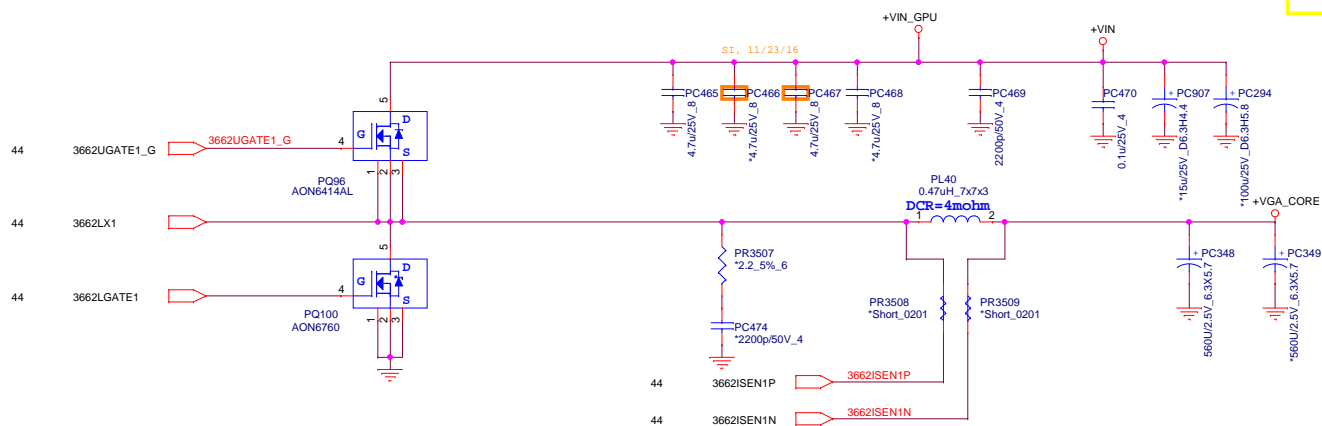
VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

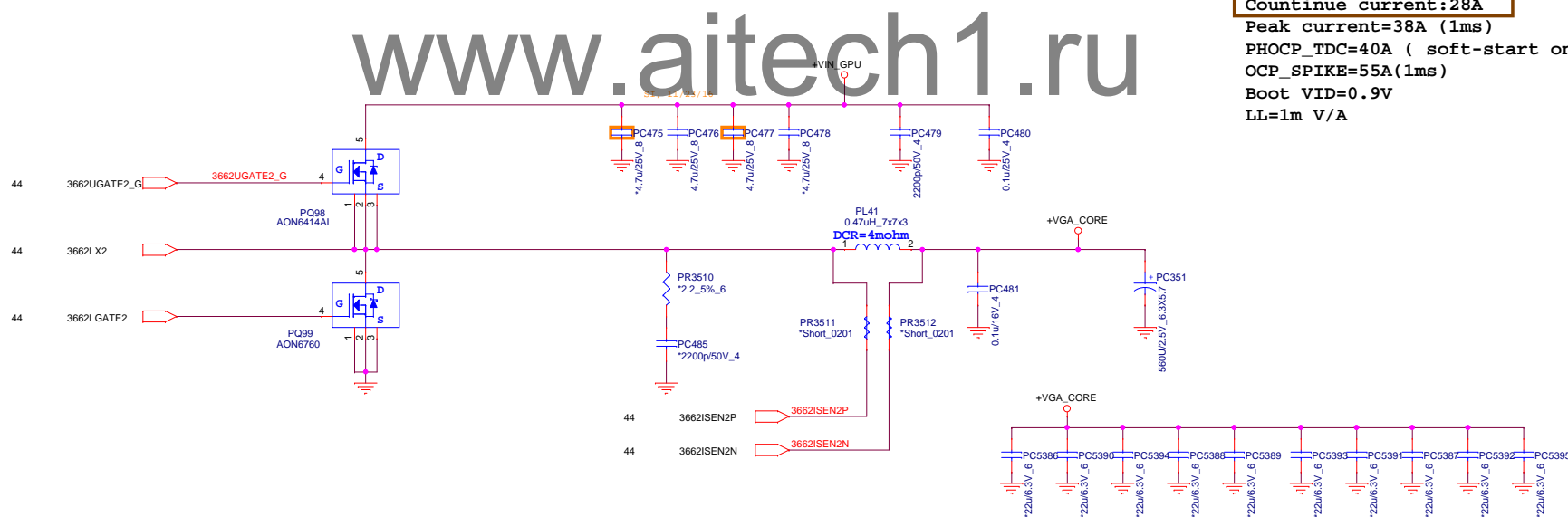
	LL=0	LL=1
Ra	14.7k	48.7k
Rb	8.66k	2.94k
Rc	27.4k	56.2k



Default M1-30
 VGACORE (R17M-M1-30_18W/25W(1ms))
Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=0m V/A

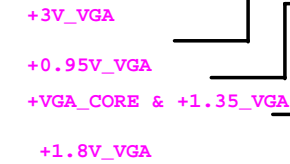
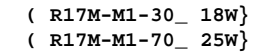


VGACORE (R17M-M1-70_25W/38W(1ms))
Countinue current:28A
 Peak current=38A (1ms)
 PHOCP_TDC=40A (soft-start only)
 OCP_SPIKE=55A(1ms)
 Boot VID=0.9V
 LL=1m V/A






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 NB5	PROJECT : Rams OP2/OP2A Quanta Computer Inc.				
	Size Custom	Document Number Storage Mode/NA			Rev 1A
	Date: Wednesday, March 08, 2017		Sheet 48 of 48		